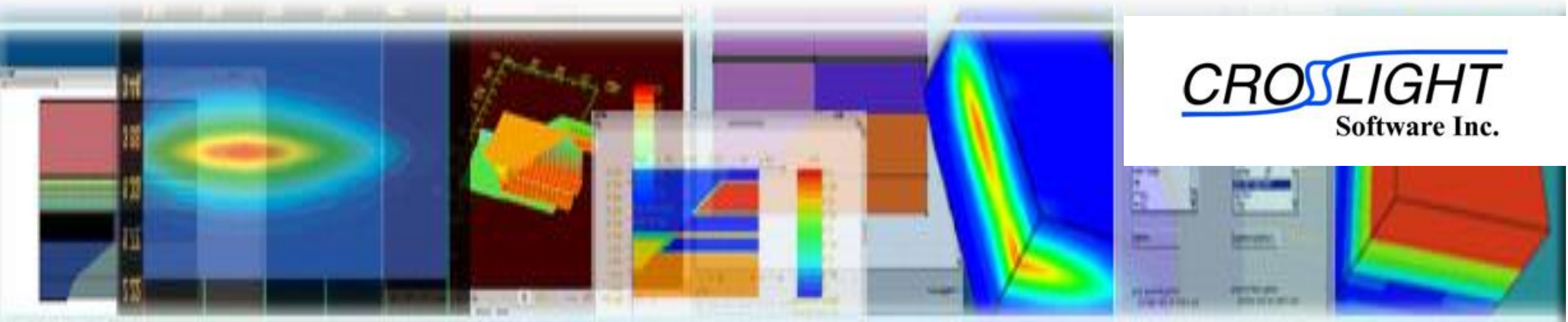


CROSSLIGHT Software Inc.

Lighting Up Semiconductor World…

APSYS | CSUPREM | LASTIP | PICS3D | PROCOM | CROSSLIGHTVIEW

3D Thin Film Transistor Simulation

Contents

1. Introduction

Amorphous silicon thin film transistors (a-Si:H TFTs) have been widely used in the active-matrix flat panel display due to the low process temperature, uniform device characteristics over large area and low fabrication cost .

3D simuation of TFT is carried out by Maskeditor, CSUPREM and APSYS.

- **MaskEditor is used to generate mask layers. Commands for use by subsequent tools may be added to each layer to generate the device structure.**
- **CSUPREM is used to generate the device structure based on the commands defined by MaskEditor. Process simulation may also be performed without using MaskEditor.**
- **APSYS is used to simulate the electrical and optical properties of the TFT device. Stand-alone device simulation may also be performed.**

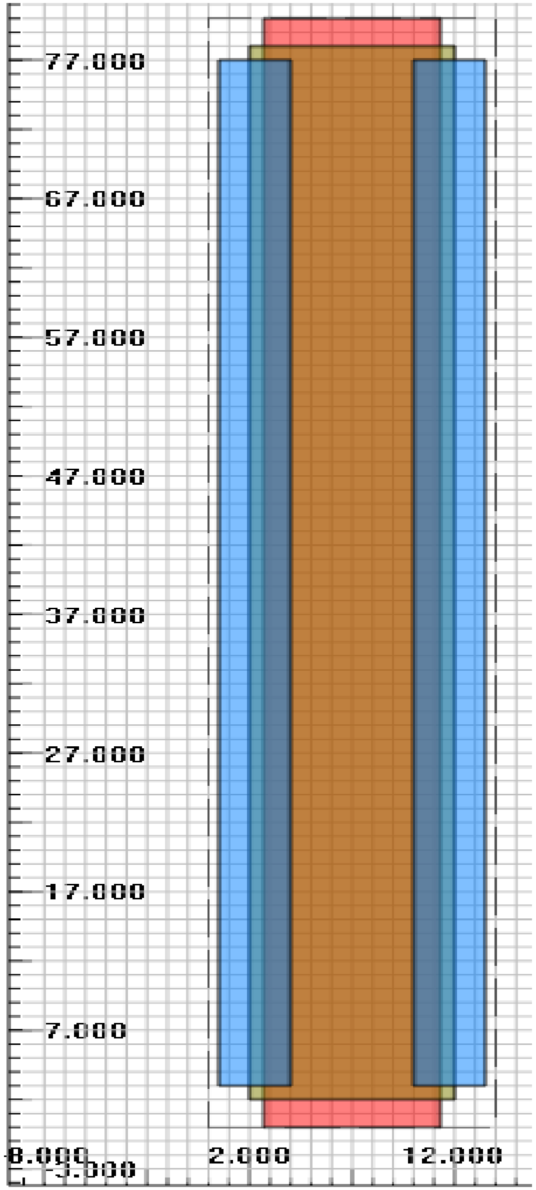
2. Process simulation

TFT mask patterns defined in MaskEditor:

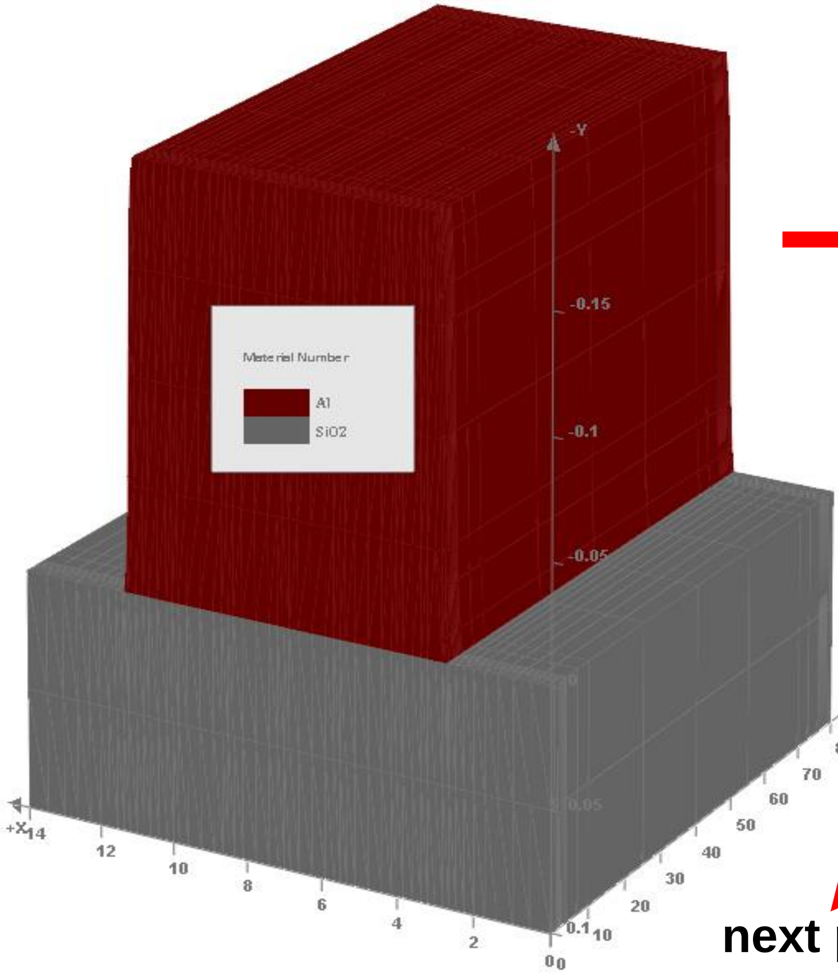
•Red mask is used to etch the gate.

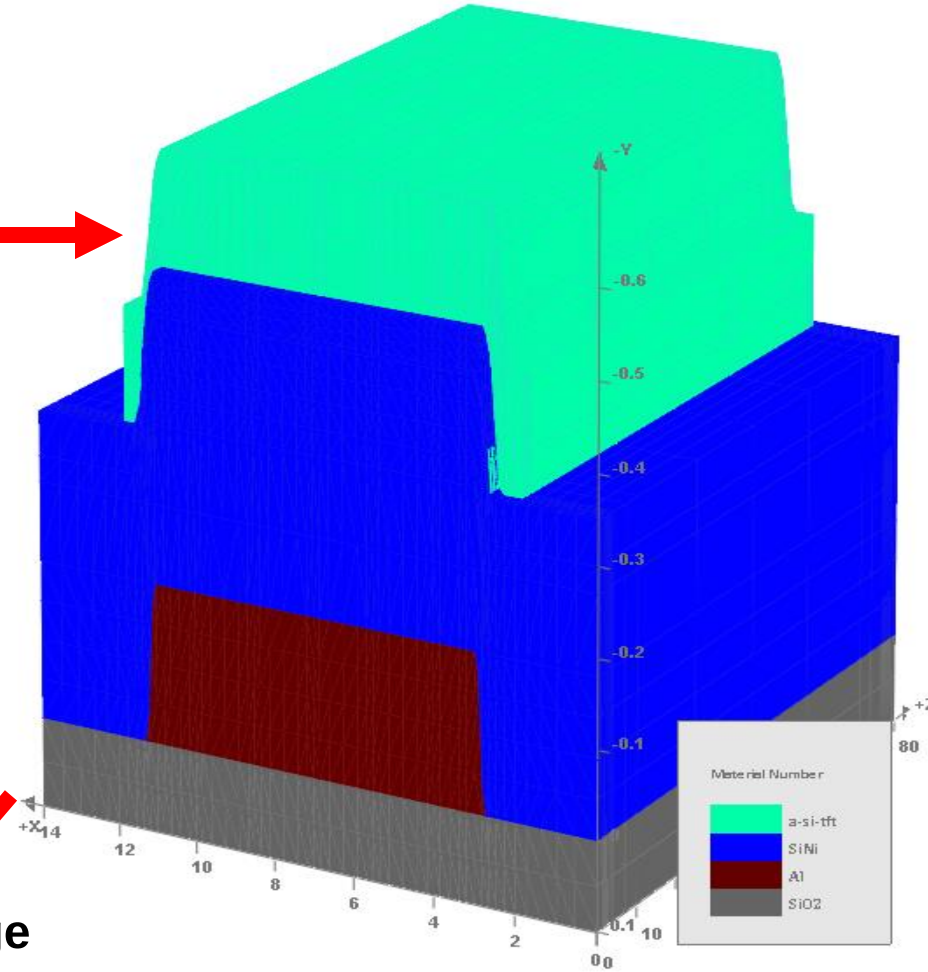
•Brown mask defines the active part.

•Blue mask used to generate the contact.



2. Process simulation



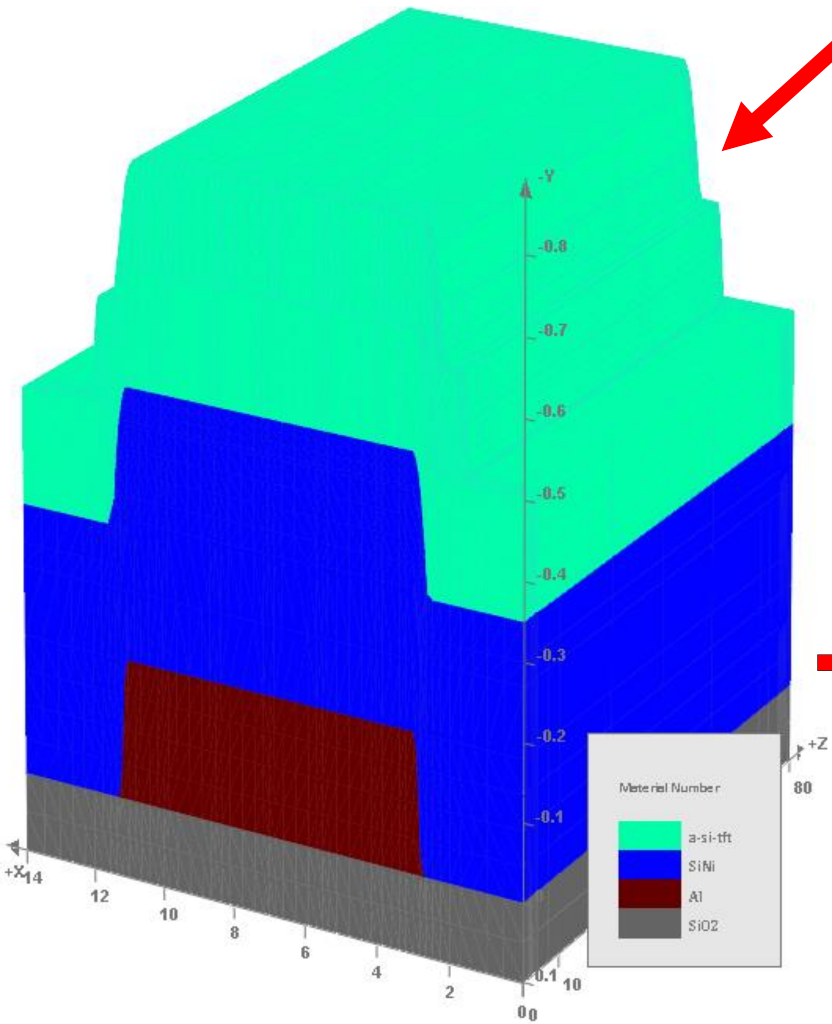


next page

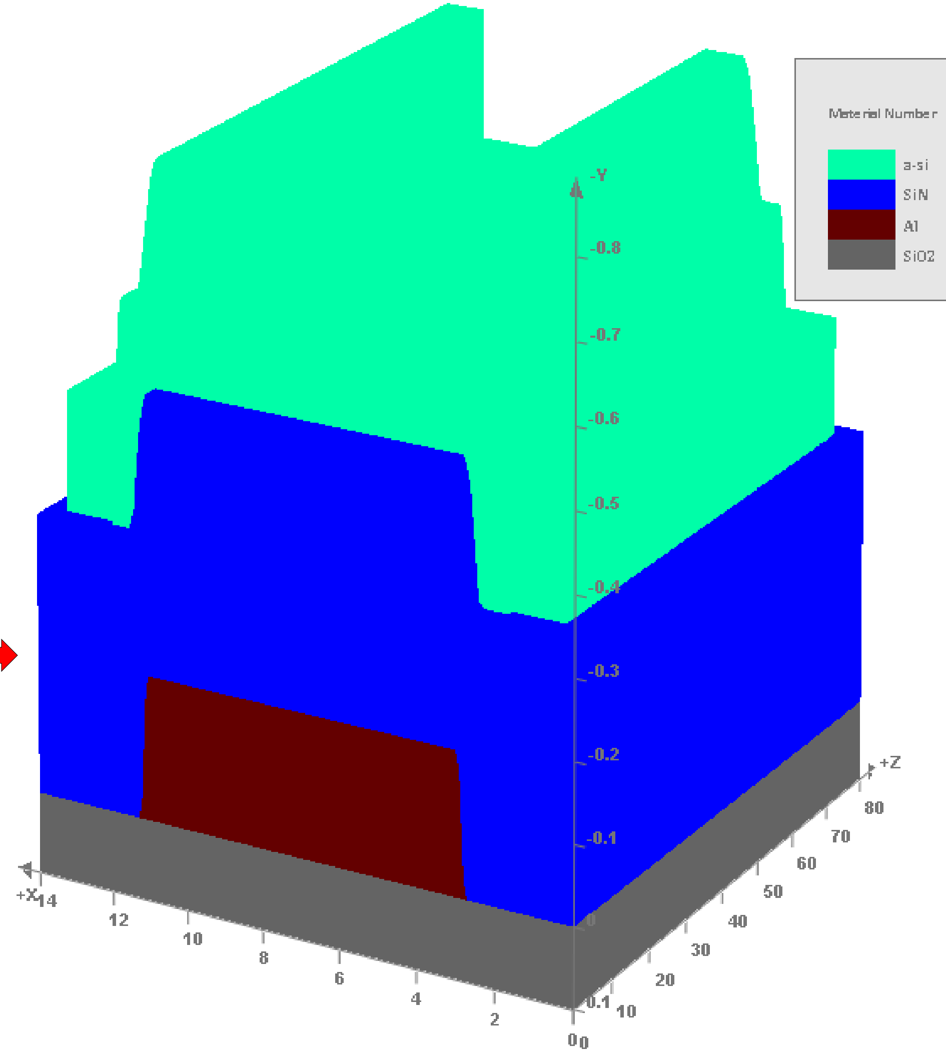
In order to view structure clearly, the SiO_2 thickness is limited to 0.1 μm. Aluminum is then deposited with a thickness of 0.18 μm and the red mask is then used to generate the gate.

The next step is to deposit 0.35μm of SiN and 0.13μm of intrinsic a-si. The brown mask is then used to generate the active area.

2. Process simulation



Deposition of 0.15µm a-si with a resistivity of 30Ω*cm.

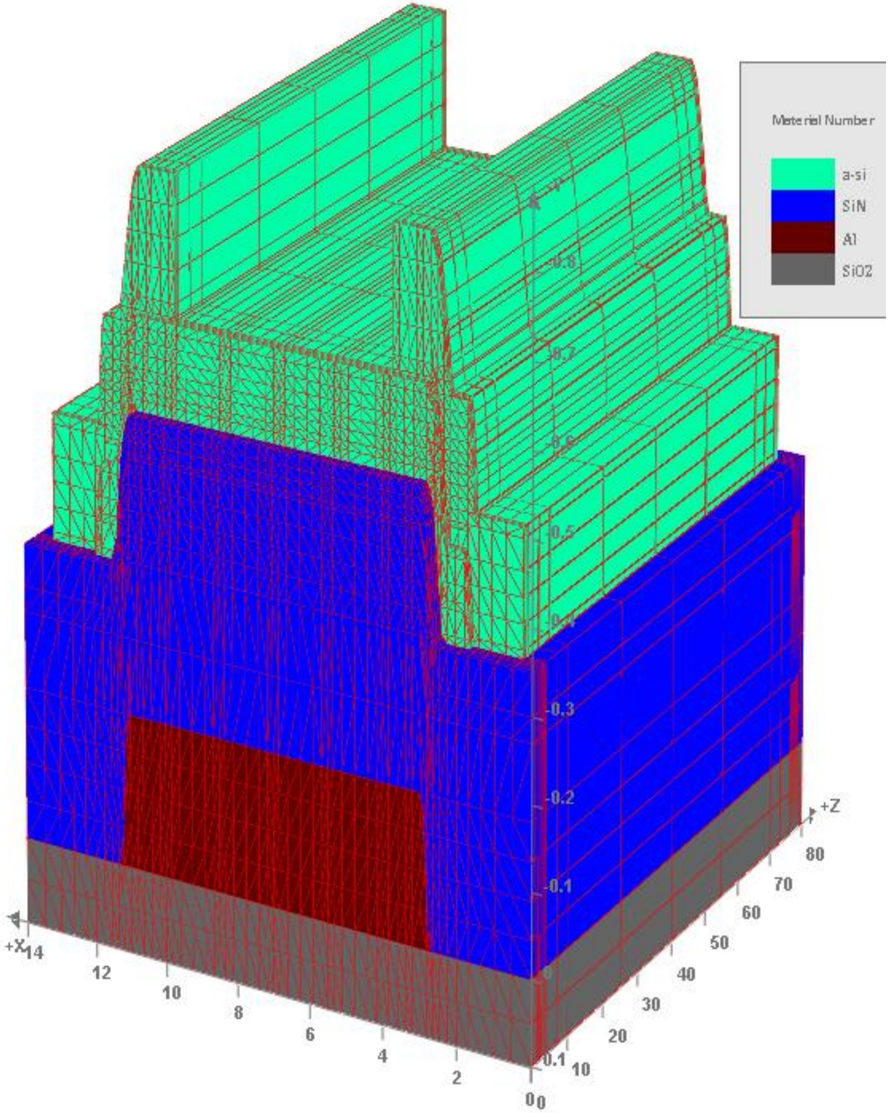


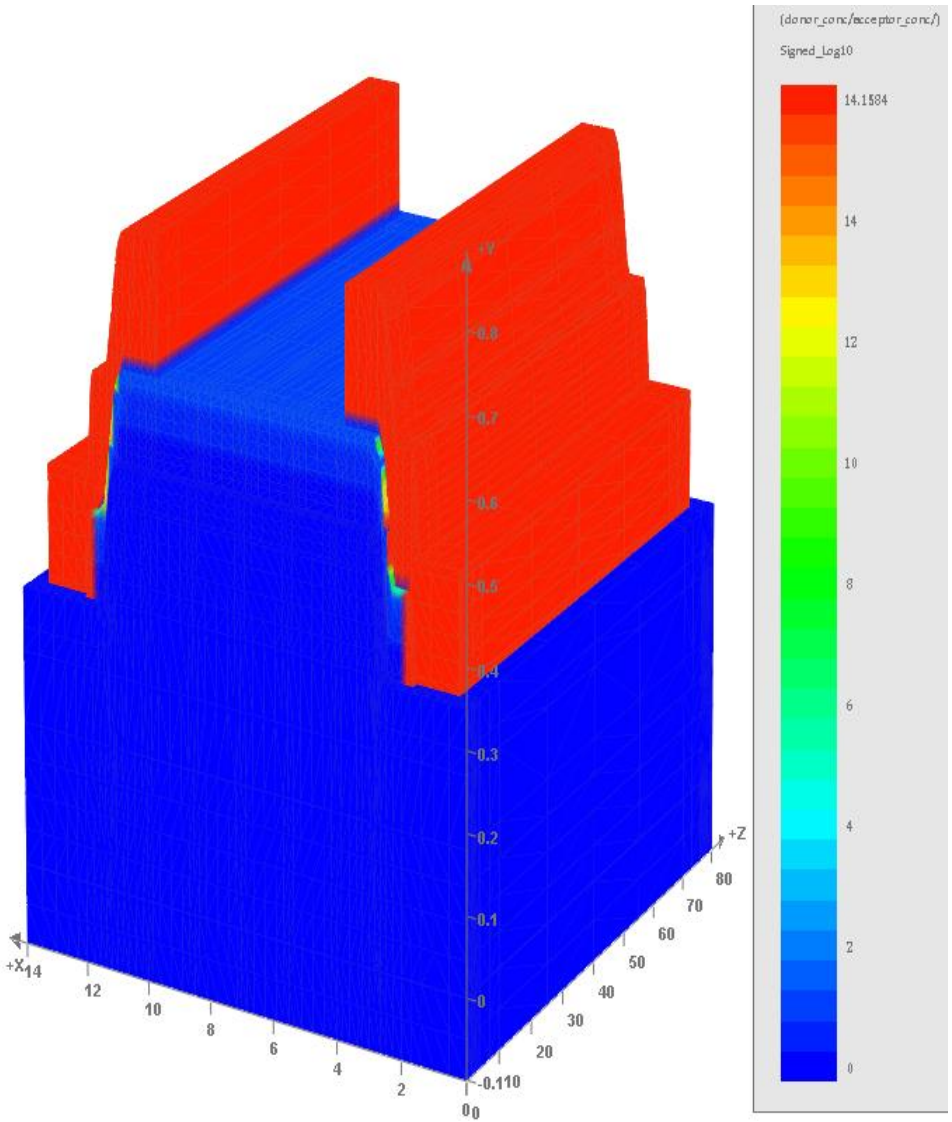
Generation of the contact with the blue mask.

CROSSLIGHT Software Inc.

2. Process simulation

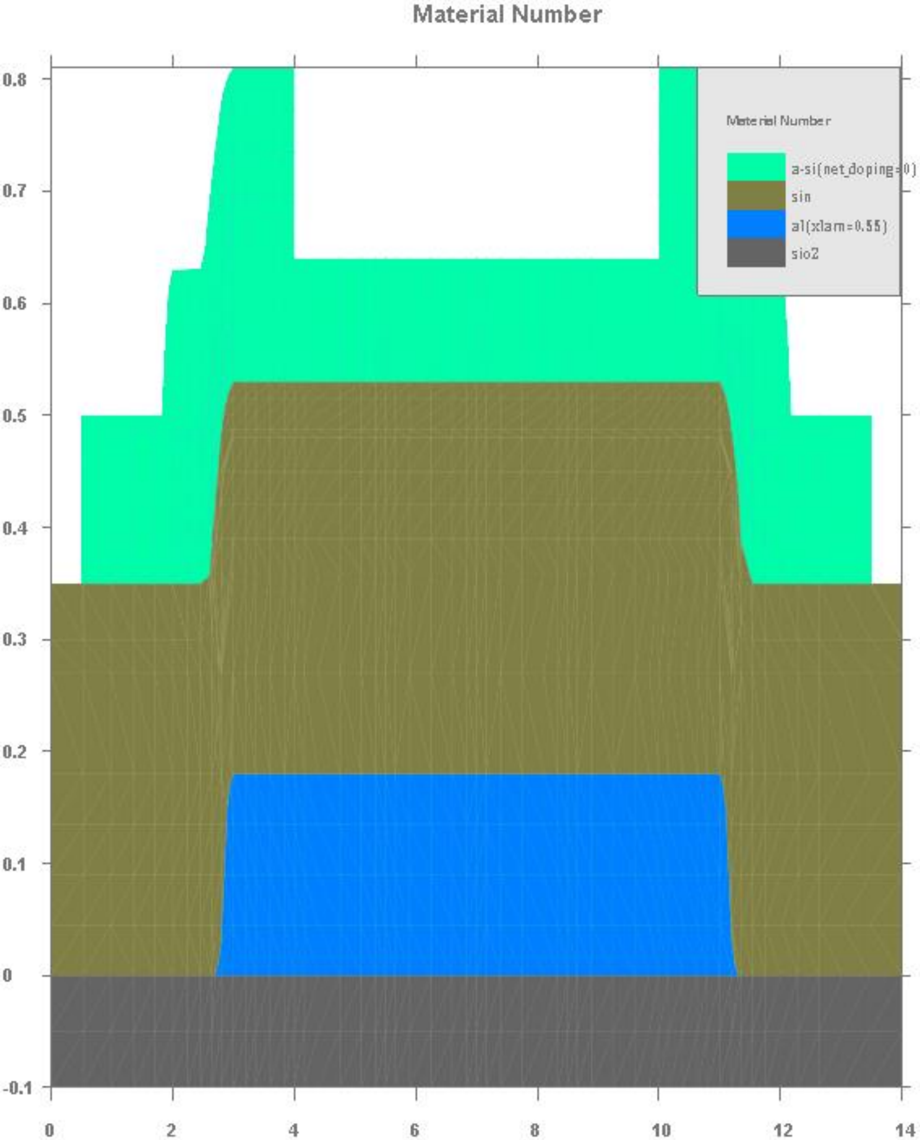
Mesh and doping profile of the device

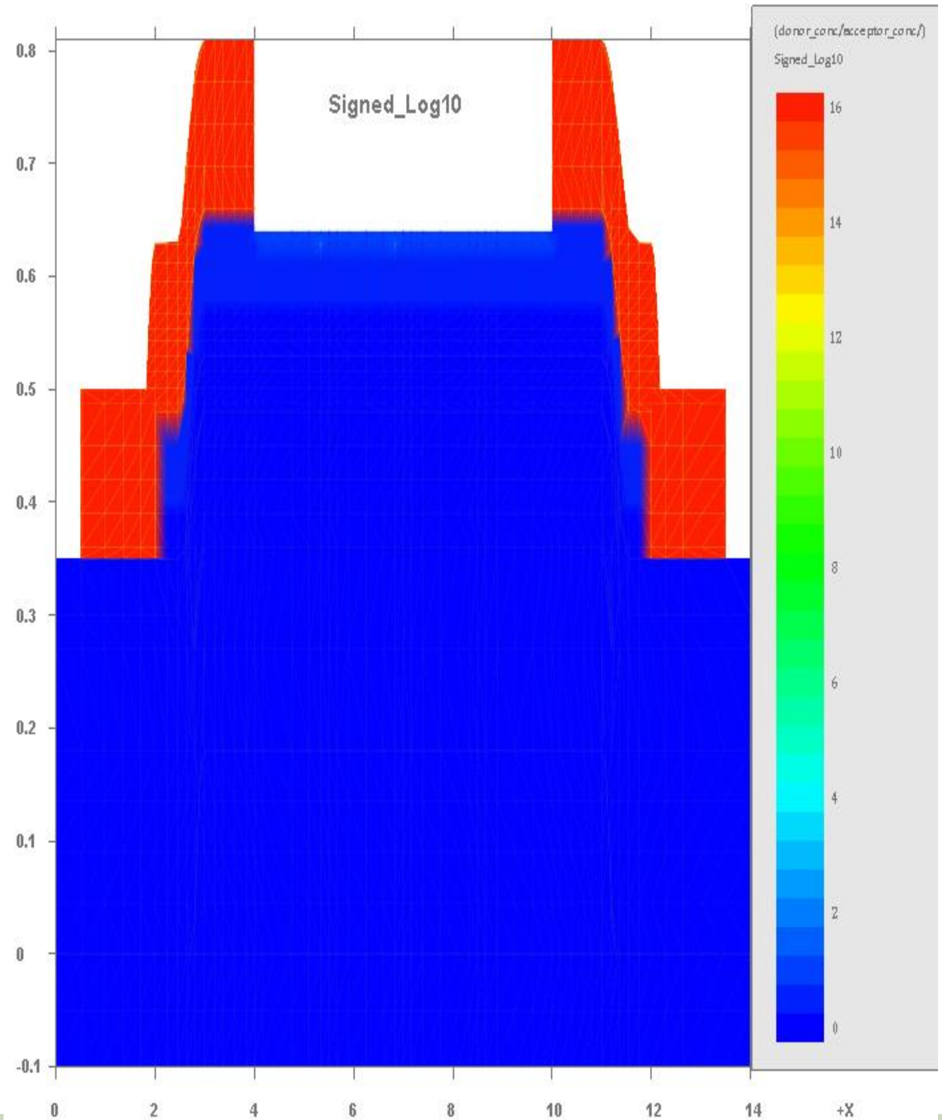




2. Process simulation

2D cut of structure and doping profile at z=40μm.





3. Physical models and parameters

Doping-dependent carrier mobilities in simulation are defined by:

$$\mu_{0n} = \mu_{1n} + \frac{(\mu_{2n} - \mu_{1n})}{1 + \left(\frac{N_D + N_A + \sum_j N_{tj}}{N_{rn}}\right)^{\alpha_n}}$$

$$\mu_{0p} = \mu_{1p} + \frac{(\mu_{2p} - \mu_{1p})}{1 + \left(\frac{N_D + N_A + \sum_j N_{tj}}{N_{rp}}\right)^{\alpha_p}}$$

electron_mass value=0.76*m_e
hole_mass value=2.52*m_e
max_electron_mob(μ_{2n}) value=20.e-4 m^2/(V*s)
min_electron_mob (μ_{1n}) value=1.e-4 m^2/(V*s)
max_hole_mob (μ_{2p}) value=5.e-4 m^2/(V*s)
min_hole_mob (μ_{1p}) value=1.e-4 m^2/(V*s)

3. Physical models and parameters

Trap settings are essential for modeling of a-Si devices. Four kinds of traps are used here:

trap_conc_2 value=1.e23 /m^3
traplevel_tail_2 value=0.05 eV
trap_ncap_2 value=2.e-21 m^2
trap_pcap_2 value=5.e-20 m^2

trap_conc_3 value=1.e23 /m^3
traplevel_tail_3 value=0.05 eV
trap_ncap_3 value=5.e-20 m^2
trap_pcap_3 value=2.e-21 m^2

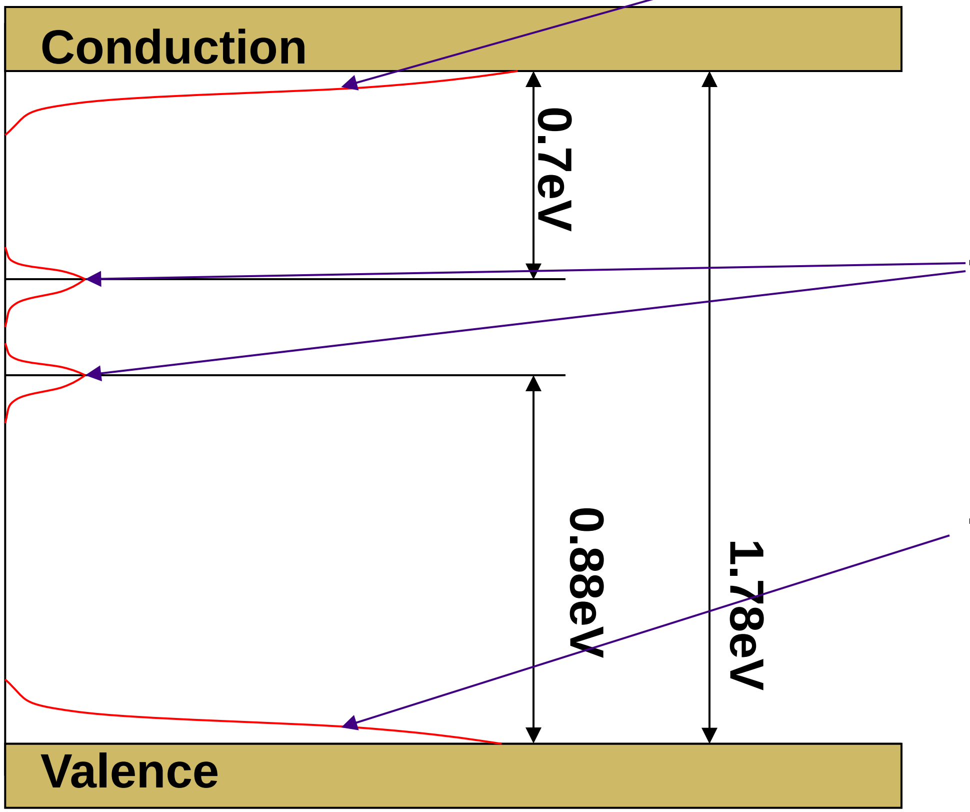
trap_conc_4 value=1.e22 /m3
traplevel_stddev_4 value=0.1 eV
trap_ncap_4 value=2.e-21 m^2
trap_pcap_4 value=5.e-20 m^2

trap_conc_5 value=1.e22 /m3
traplevel_stddev_5 value=0.1 eV
trap_ncap_5 value=5.e-20 m^2
trap_pcap_5 value=2.e-21 m^2

3. Physical models and parameters

Trap Models

•Traps labeled #2 and #4 are acceptor levels.
•Traps labeled #3 and #5 are donor traps.



Trap_2:
- Due to broadening of the conduction band.
- Energy level has an exponential tail.

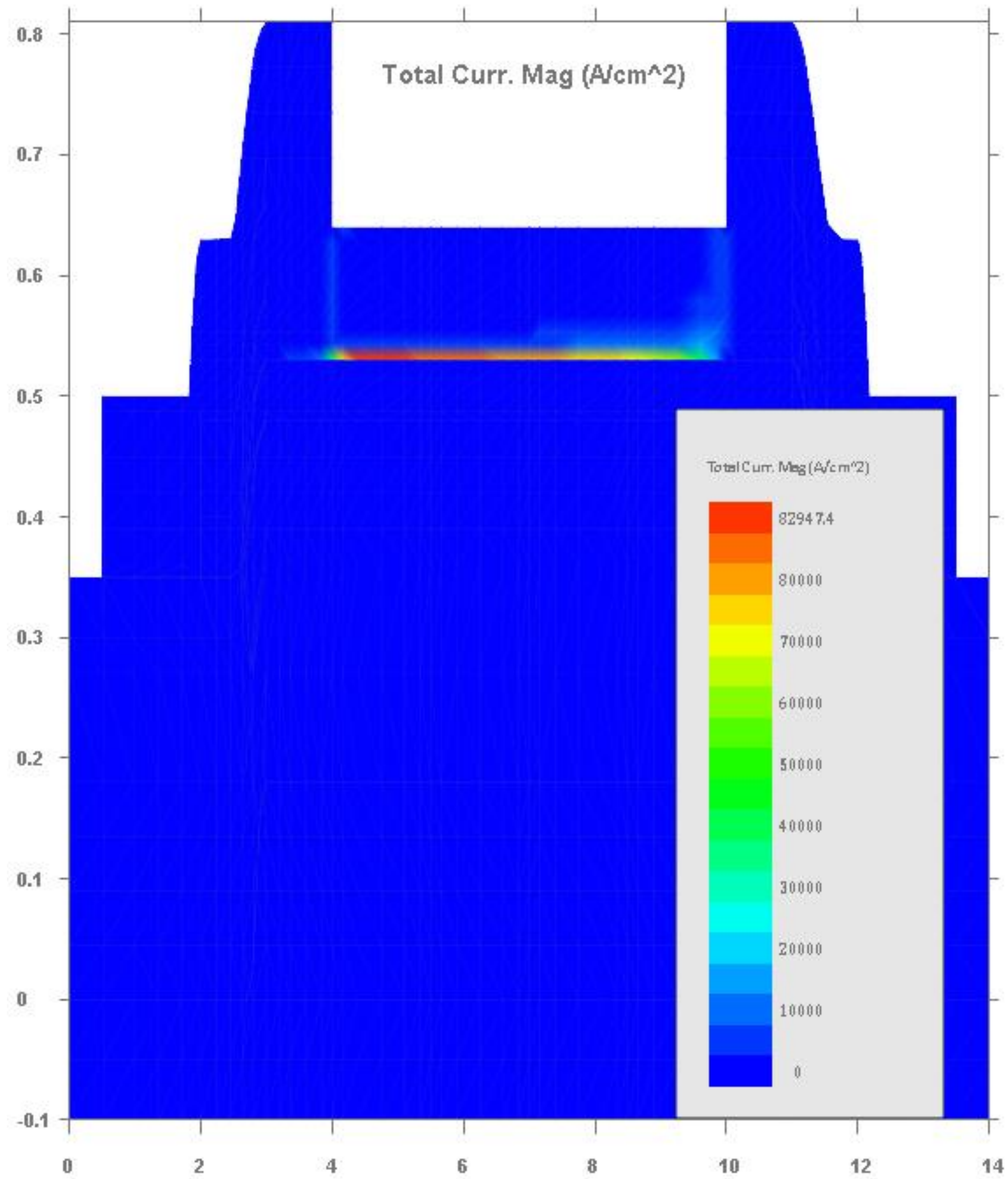
Trap_4 & Trap_5 :
- Due to dangling Si-Si bonds.
- Energy level has a Gaussian distribution.

Trap_3:
- Due to broadening of the valence band.
- Energy level has an exponential tail.

4. Results

Current density distribution

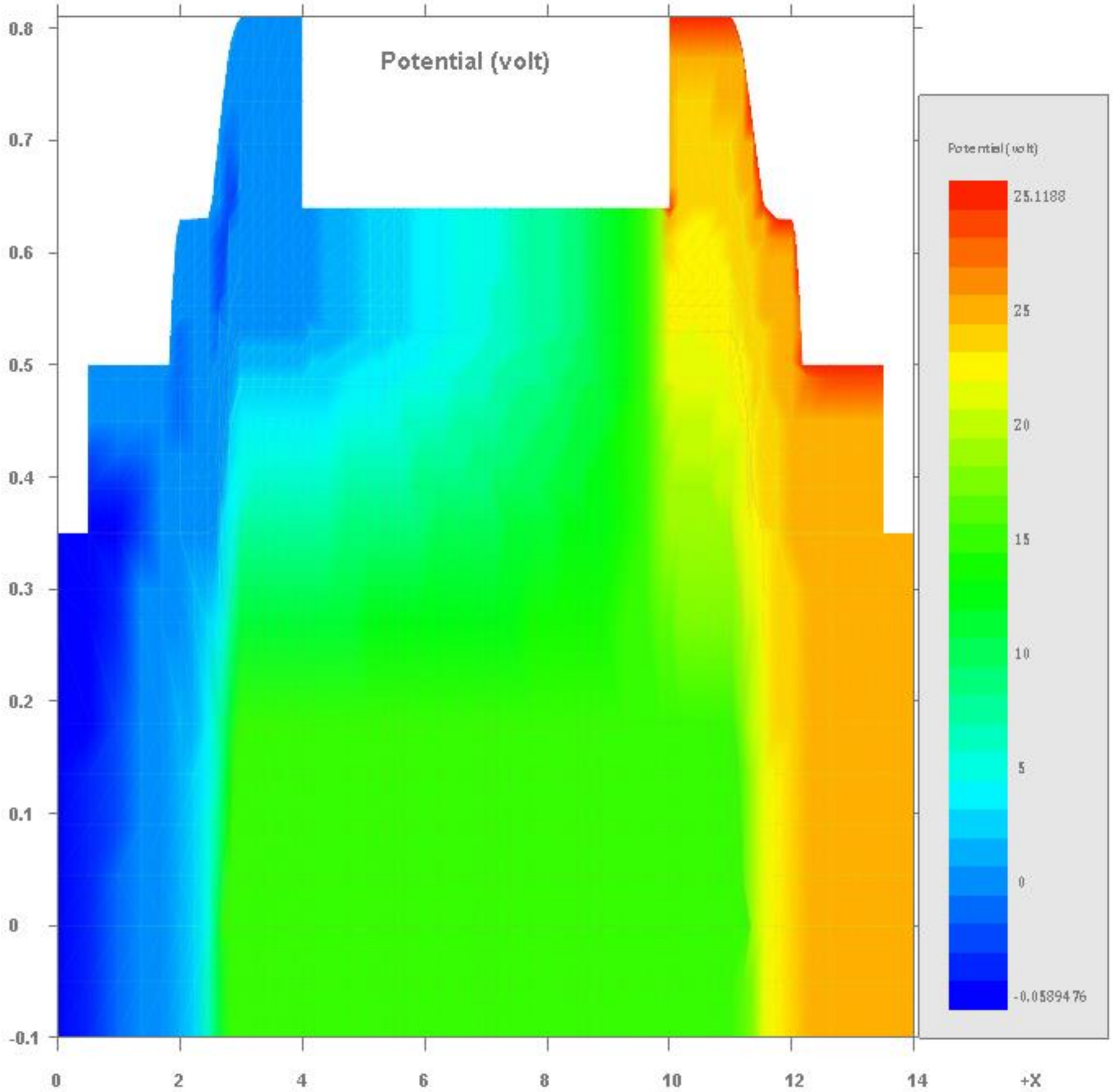
@ gate voltage=15 V
@ drain voltage=25 V



4. Results

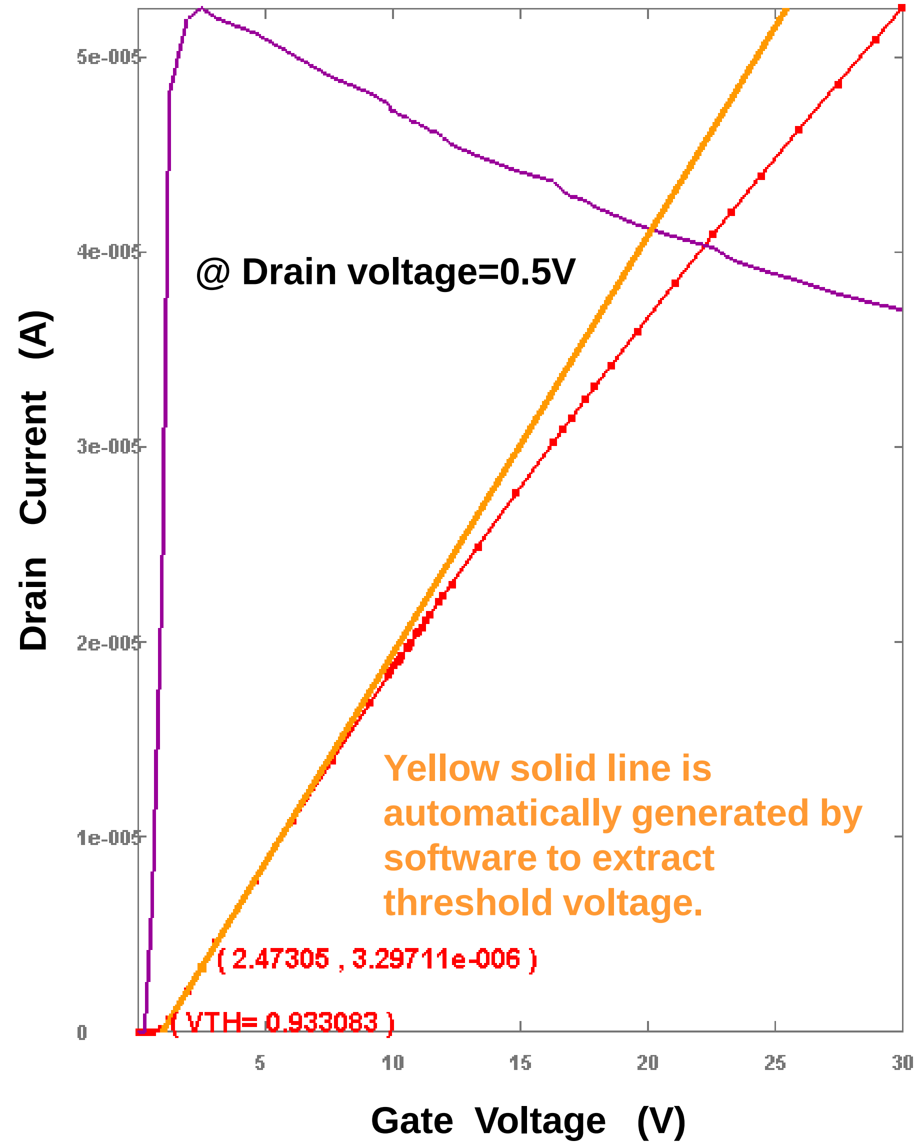
Potential distribution

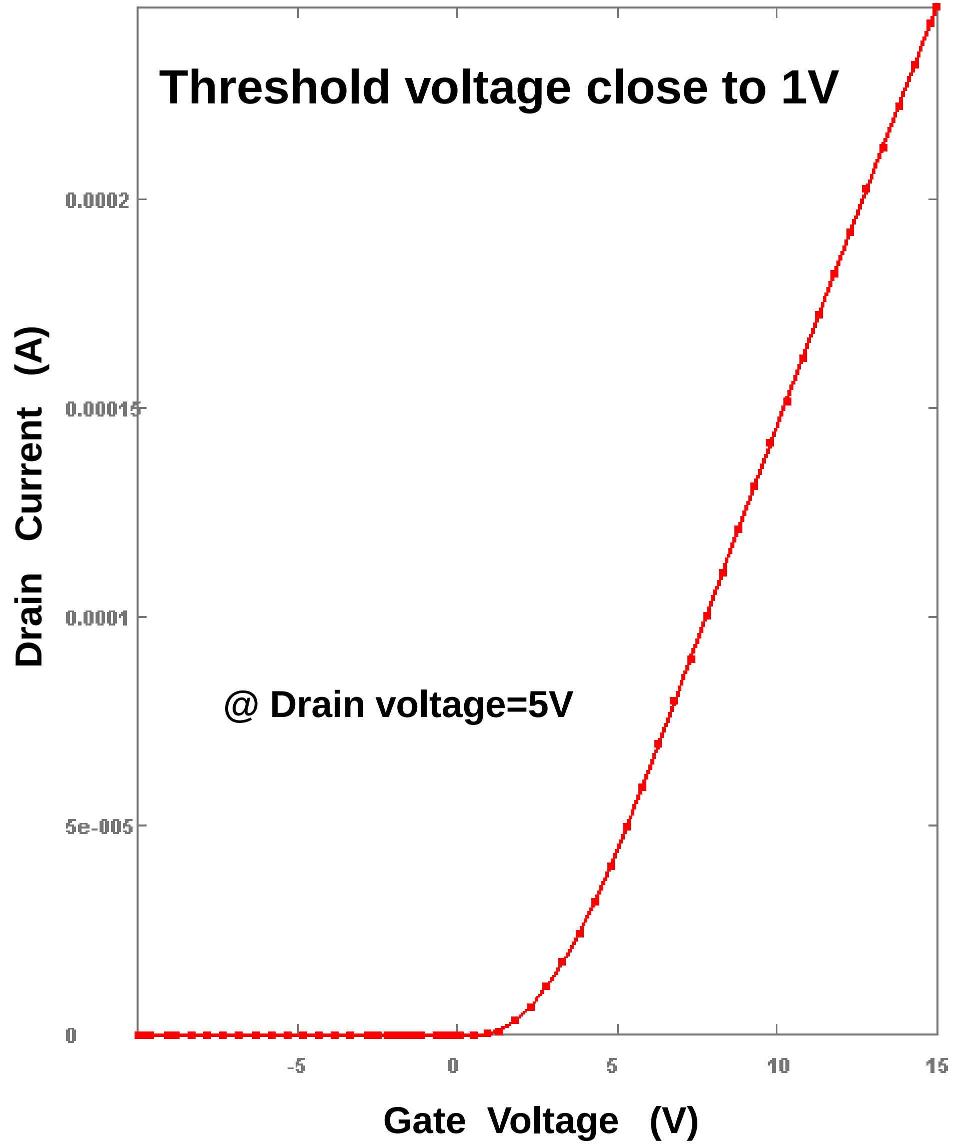
@ gate voltage=15V
@ drain voltage=25V



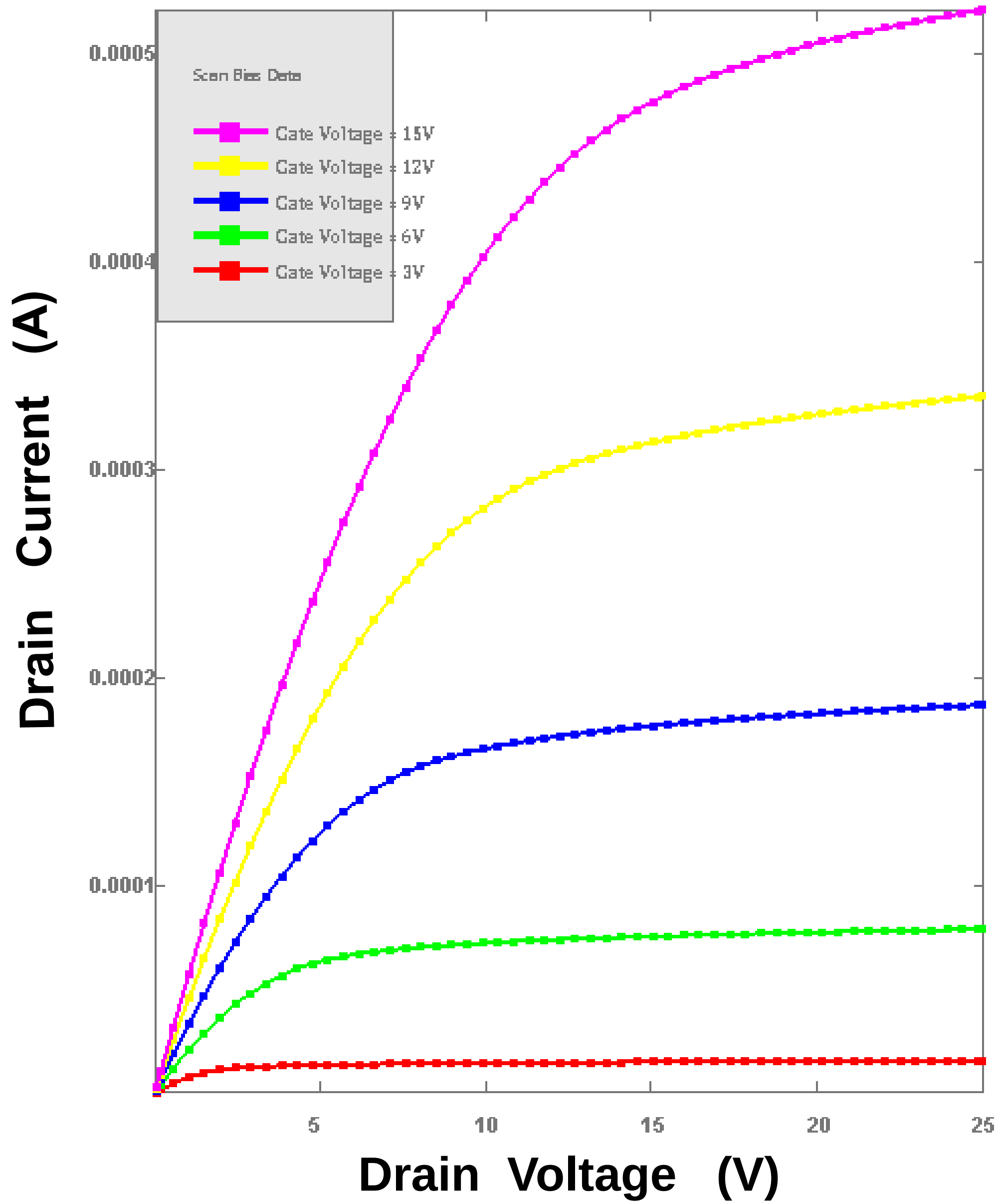
4. Results

Threshold voltage





4. Results



Id-Vd family of curves

Creators of Award Winning Software

CROSSLIGHT Software Inc.