Simulation of 3D Effects in MOSFET Using CSuprem3D and Apsys3D

CROSSLIGHT Software Inc.

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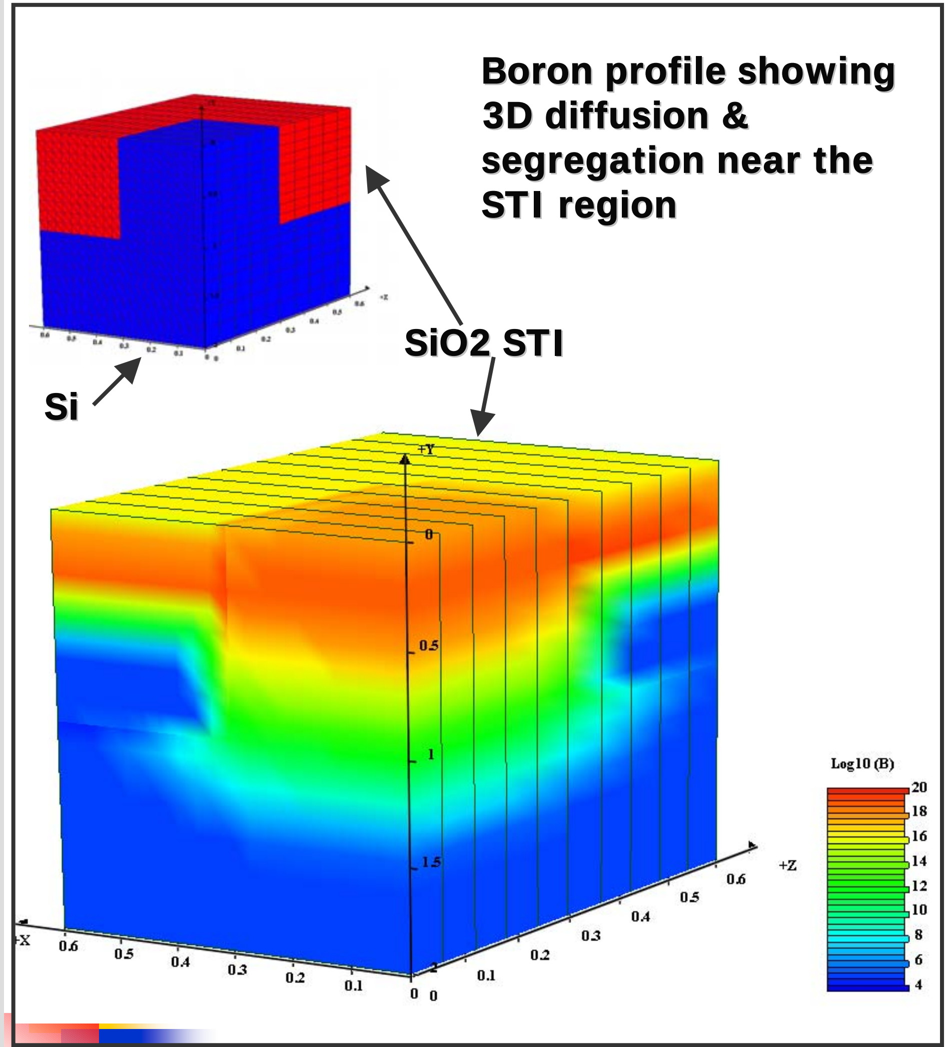
Contents

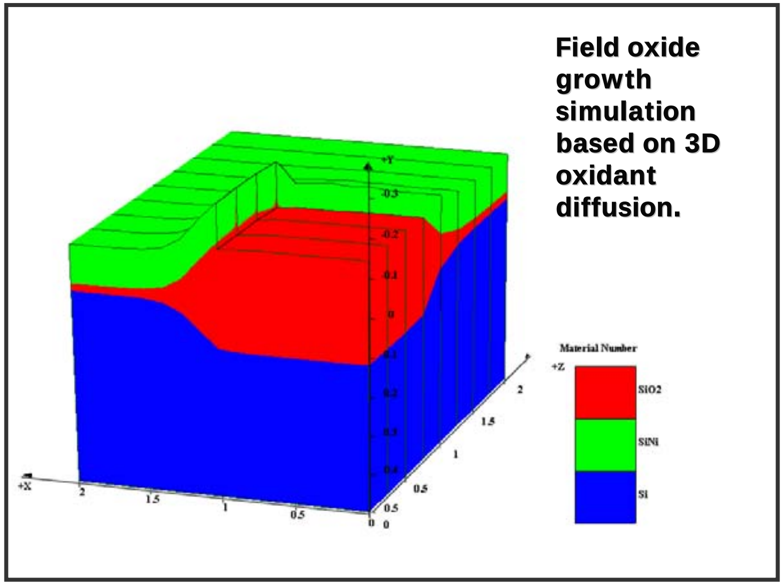
- General overview of CSuprem
- 3D width effect in HV-MOSFET
- 3D width effect in nano-MOSFET
- 3D Trench corner effect in UMOS
- Summary

CSuprem (2/3D) -Crosslight's Advanced Process Simulator



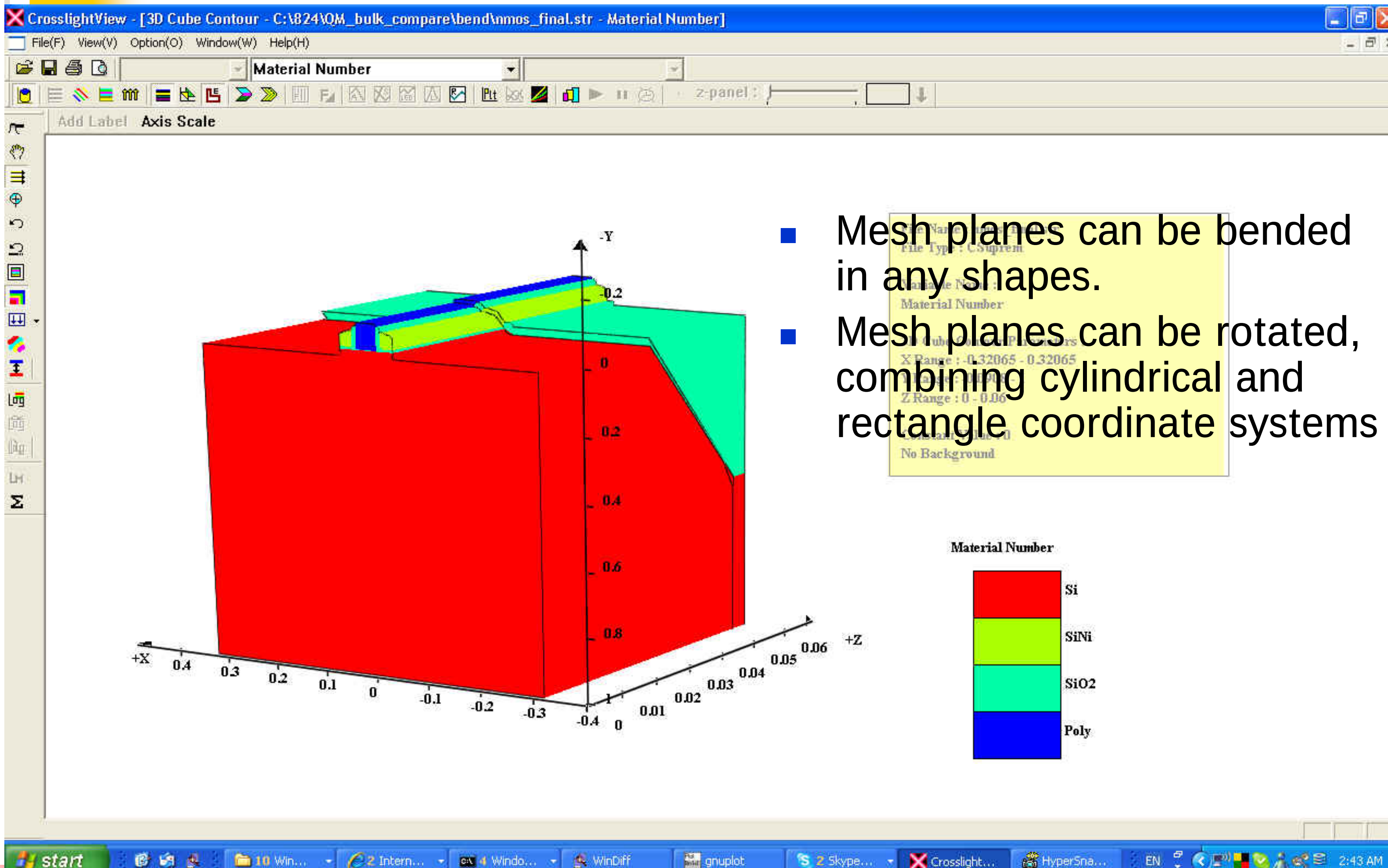
Boron profile showing 3D diffusion & segregation near the STI region

- Extension of Stanford's code to full 3D with inter-plane coupling.
- Direct use of existing 2D input decks in 3D simulation.
- Full 3D model for diffusion, segregation & oxidation.



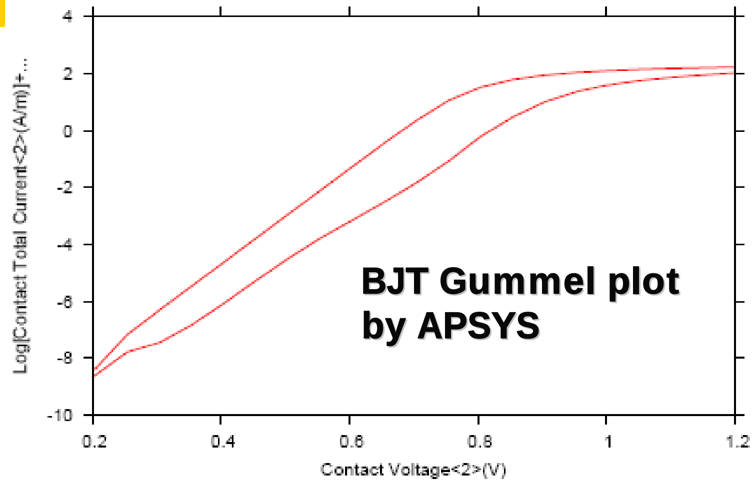
Field oxide growth simulation based on 3D oxidant diffusion.

Csuprem-3D –Flexible 3D mesh

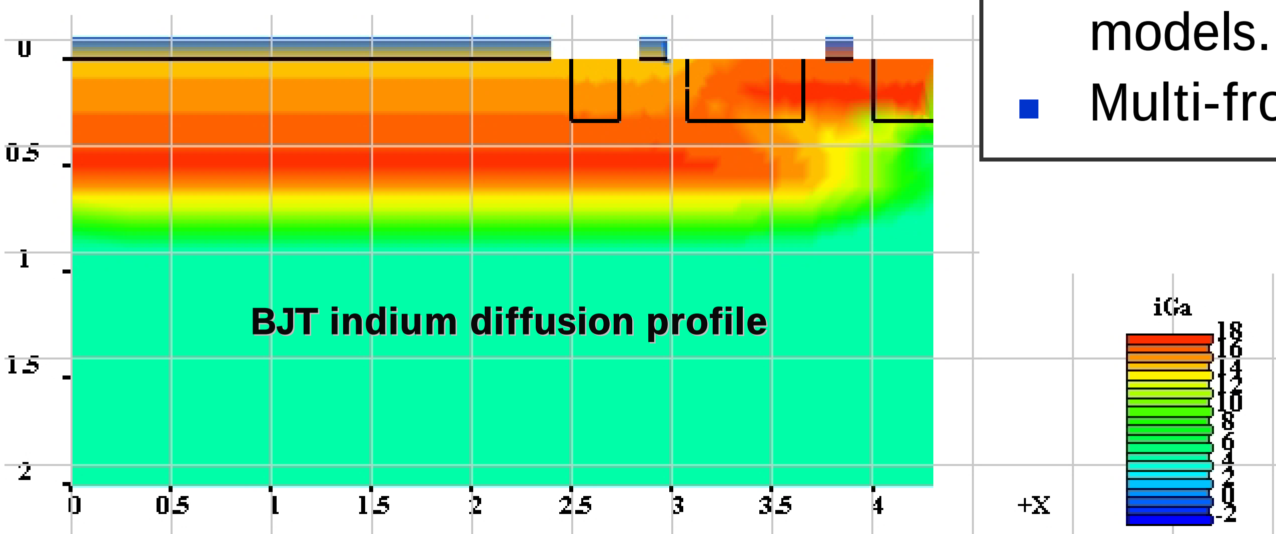


- Mesh planes can be bended in any shapes.
- Mesh planes can be rotated, combining cylindrical and rectangle coordinate systems

Advanced features of CSuprem



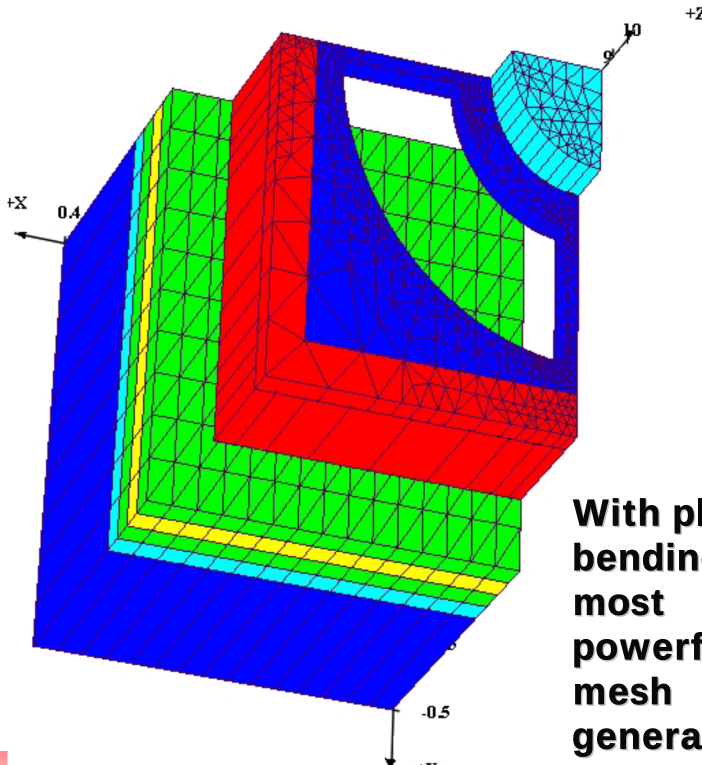
- Dual-Pearson implant table.
- SIMS/MC data import.
- RTA annealing models.
- Point-defect, TED models.
- Numerous generic impurity/material models.
- SiGe diffusion & stress models.
- Multi-frontal parallel solver.



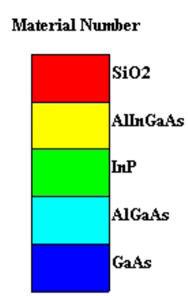
Simulation with imported longitudinal SIMS data.
Angle/lateral implant profile calculation by CSuprem

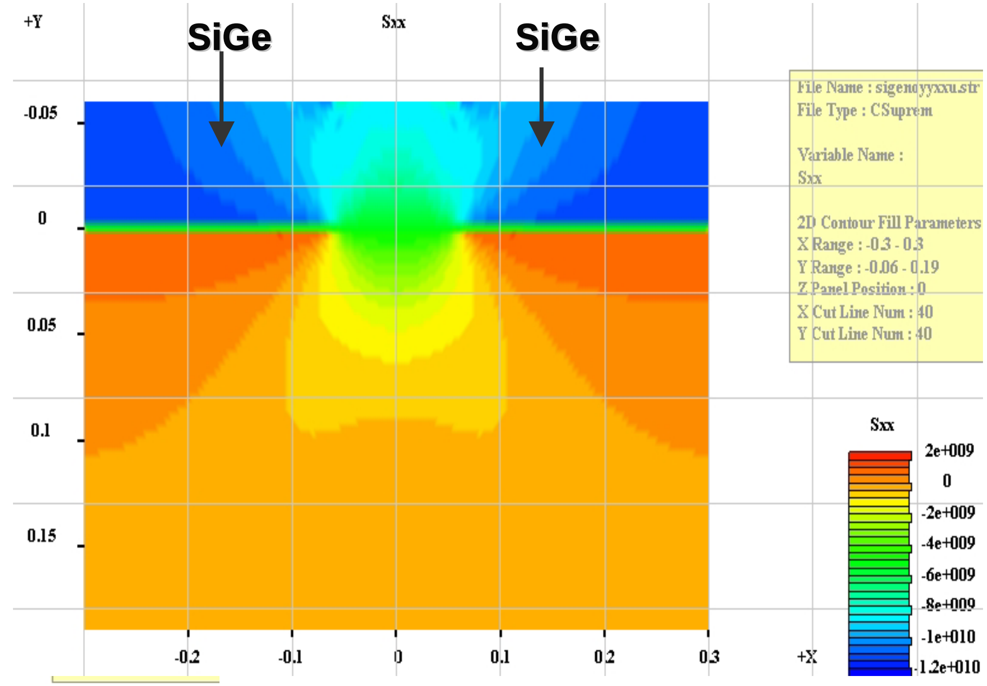
Mechanical stress/strain modeling

Simulated MEMS tunable vertical cavity semiconductor amplifier



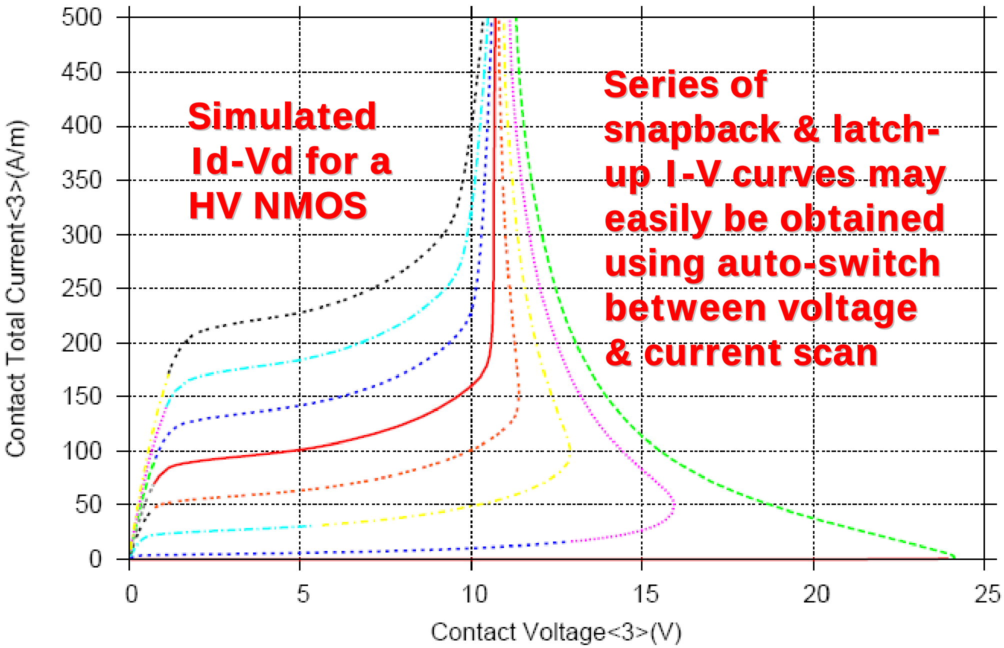
With plane-bending, most powerful 3D mesh generation

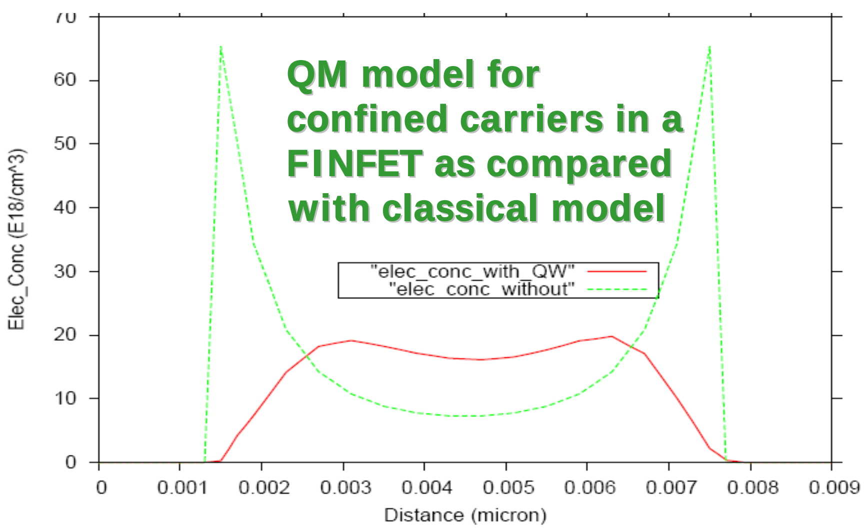




Simulated uniaxial stress profile in SiGe-PMOSFET with microscopic internal stress model.

CSuprem/Apsys Combination





CSuprem mesh & doping may be used by Crosslight's device simulator APSYS

Advanced Features of Apsys

- Robust convergence.
- Self-consistent model for QM confinement & tunneling.
- Capabilities of DC/AC, large signal, trap dynamic, hot carrier & self-heating.

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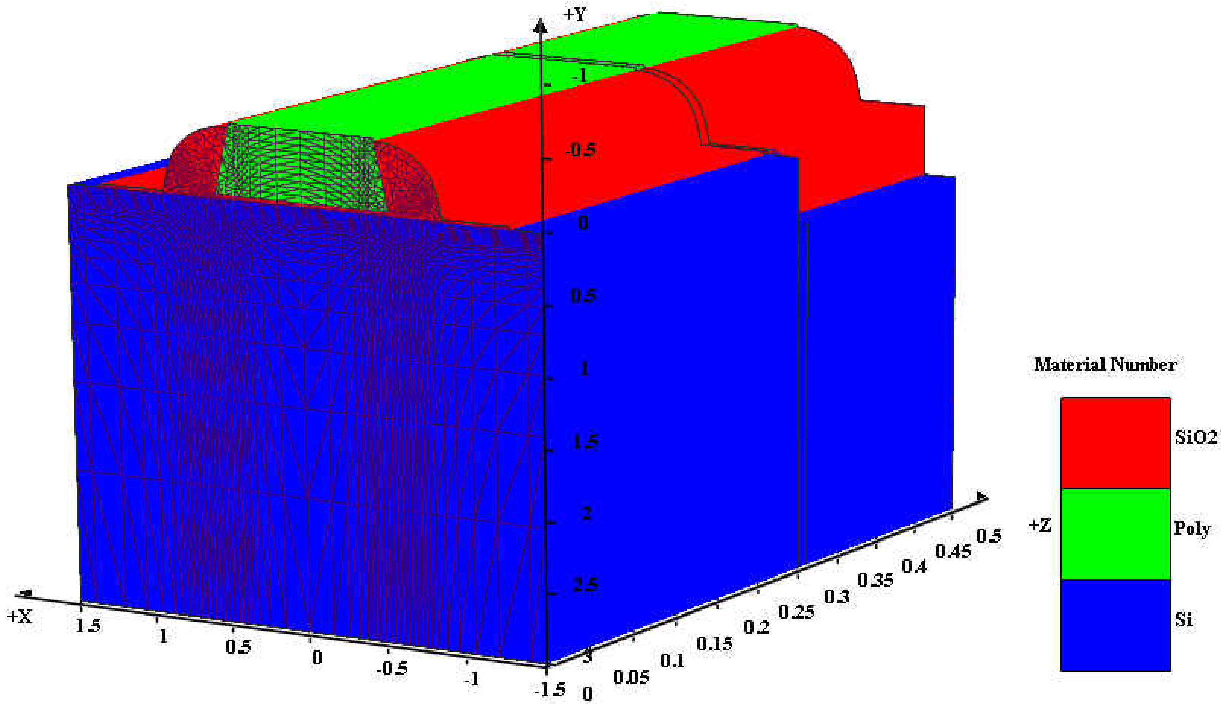
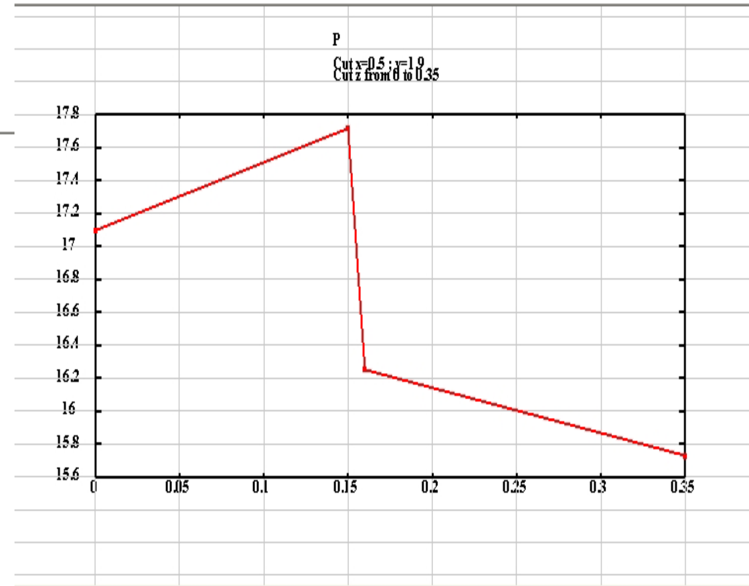
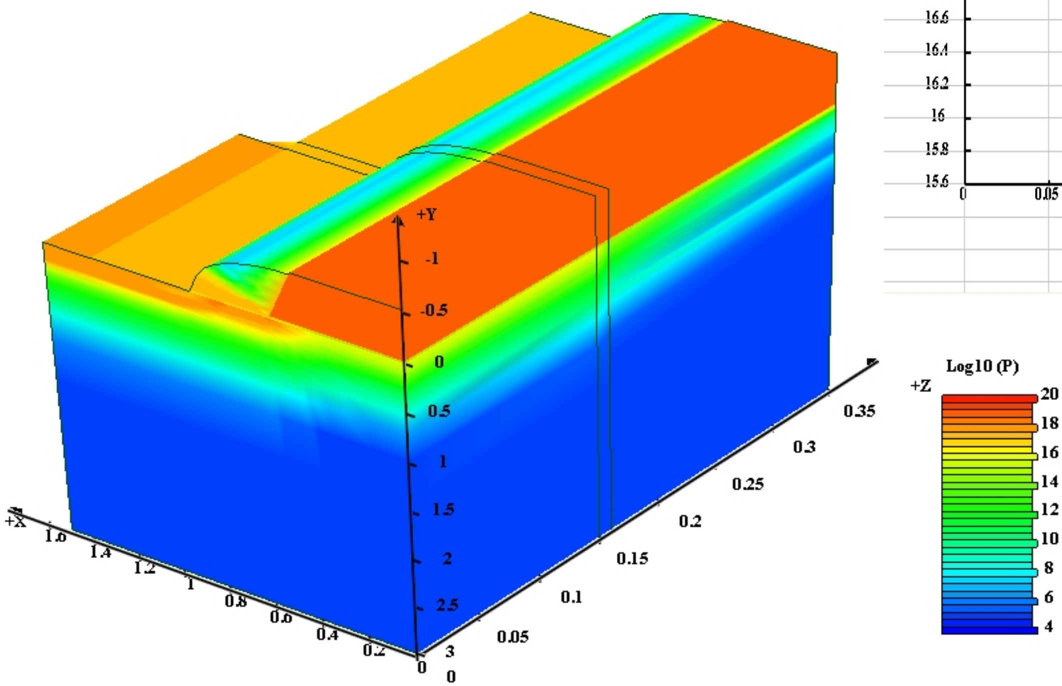
3D STI structure/process



- Standard process/structure taken from example 5 of Suprem4.gs in the original Stanford release.
- Convert into 3D using a vertical STI

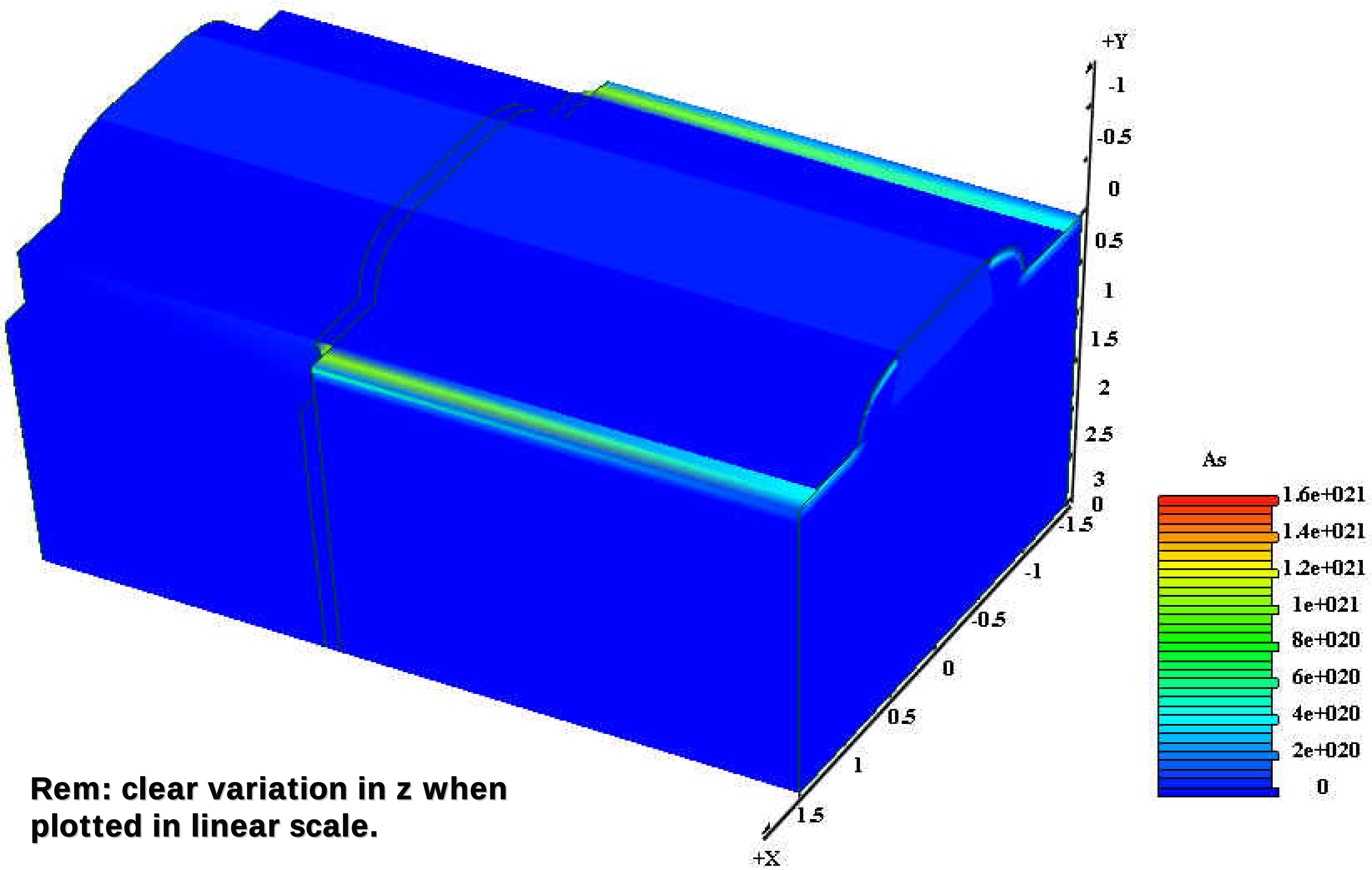
P profile (STI)





Remark: visible variation in z due to STI interface segregation/diffusion.

As profile (STI)



Rem: clear variation in z when plotted in linear scale.

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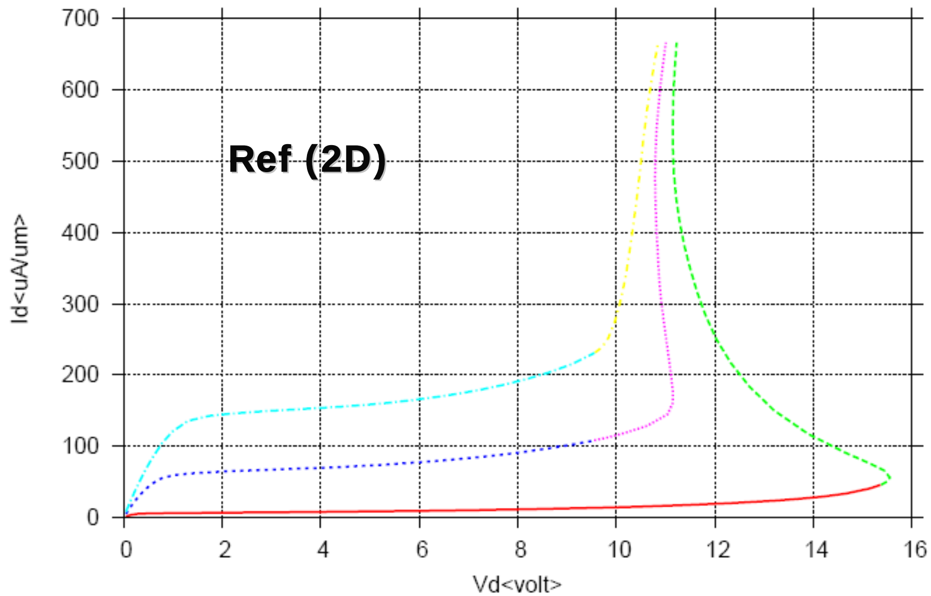
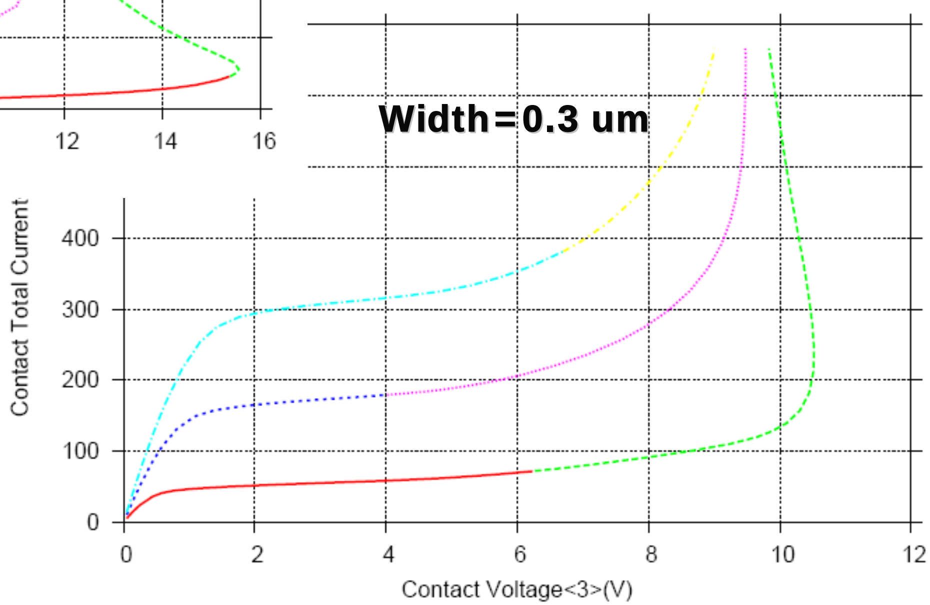
Id-Vd 2D vs. 3D





Drain current normalized to channel width (uA/um).

Vg=1,2,3 V

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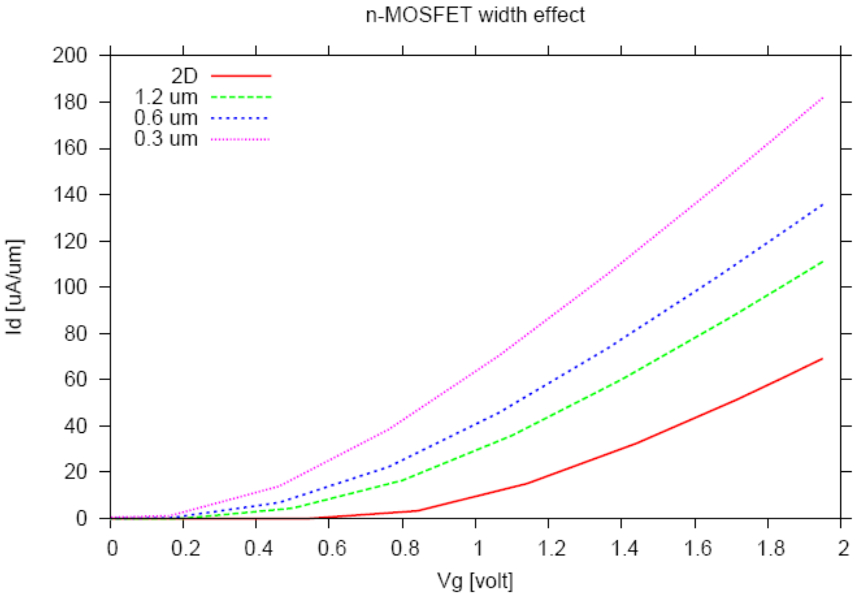
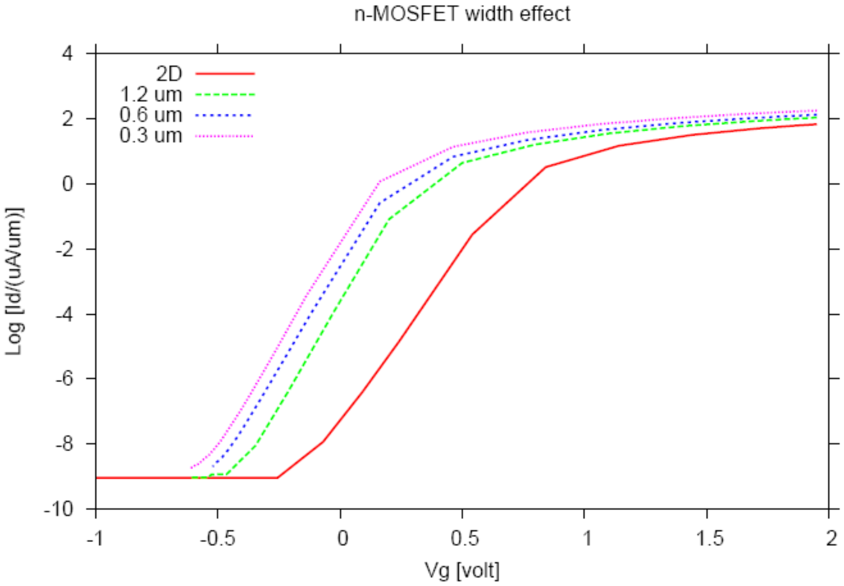
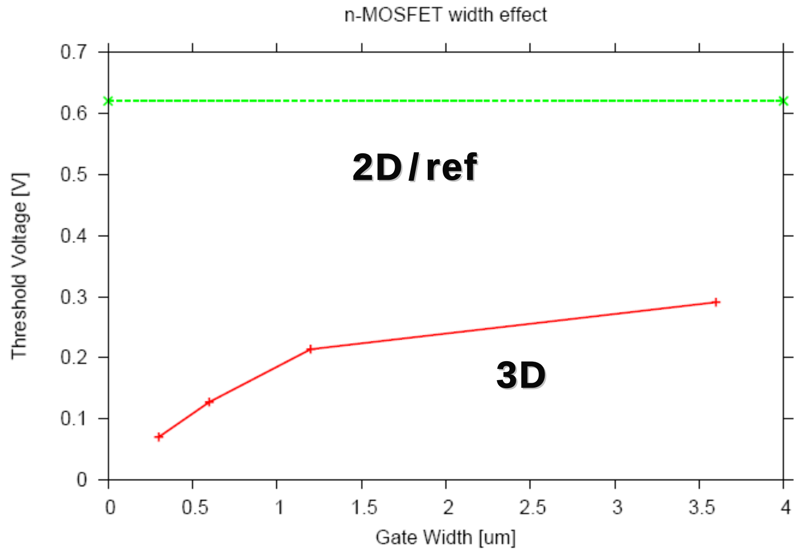
Threshold behavior





Remark: due to width diffusion/segregation effect, we see significant shift in Vt.

Threshold voltage vs. width



Experimental: Ohe et. al., IEEE EDL, vol 13, No. 12, Dec. 1992, p.636

Due to difference in structure and process condition, comparison of trend is intended.

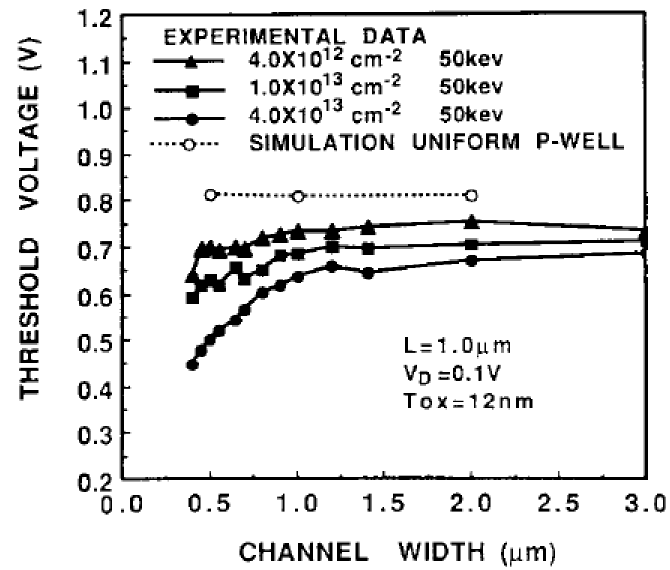


Fig. 1. Experimental data of the threshold voltage versus the channel width for three types of p-well concentration and simulation data for 1.8×10^{17} cm^{-3} uniform p-well.

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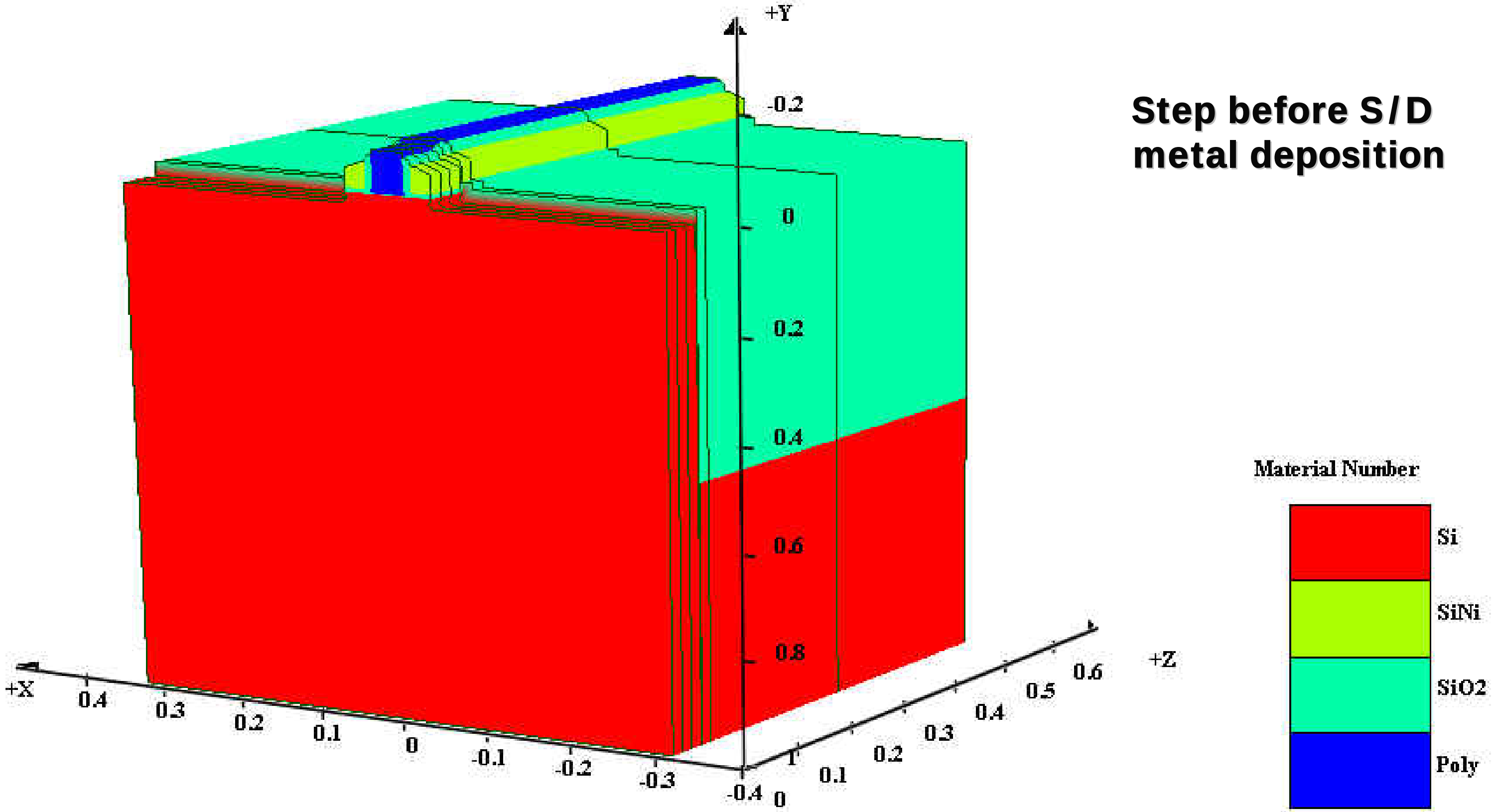
Case study for Lg=0.0413 um



Step before S/D metal deposition

Up to 8 mesh-planes are used with similar z-mesh spacing near STI interface. In the channel, z-mesh spacing is uniform while spacing in STI is adjusted to use more mesh near STI interface.

A typical Nano-MOSFET process flow

- channel implant B BF2
- anneal
- oxide 1 anneal dryo2
- oxide 2 anneal dryo2
- gate oxide deposit
- deposit poly
- poly anneal
- poly patterning
- re-oxidation anneal
- anneal
- step N Halo1: implant BF2
- step N Halo2: implant In, N
- LDD Implant As
- linear oxide anneal
- deposit nitride spacer
- etch oxide/nitride spacer
- NSD implant: As, P
- step NSD RTA anneal (*)
- step metal deposit

Full steps with all thermal cycles.

(*) RTA from 500 to 1000 C.

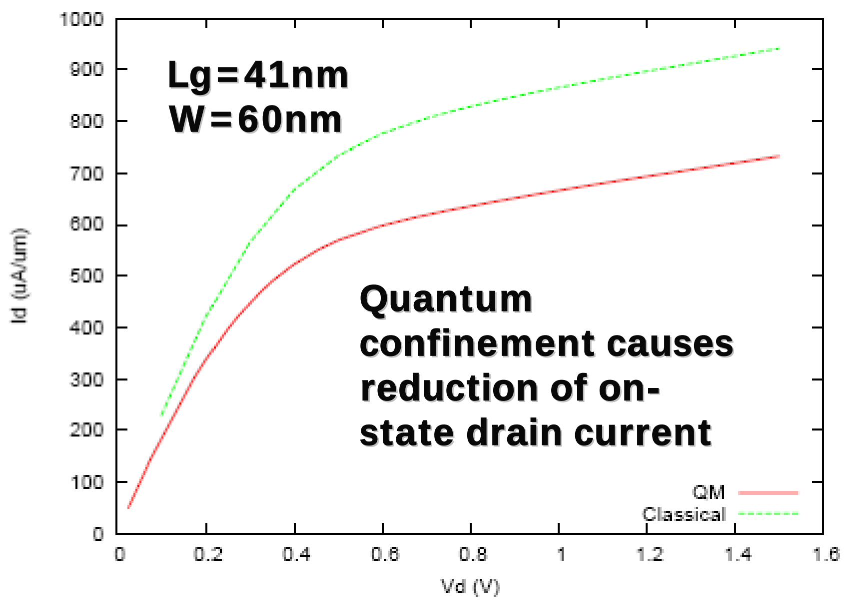
- channel implant B BF2
- #anneal
- #oxide 1 anneal dryo2
- #oxide 2 anneal dryo2
- gate oxide deposit
- deposit poly
- #poly anneal
- poly patterning
- #re-oxidation anneal
- anneal
- step N Halo1: implant BF2
- step N Halo2: implant In, N
- LDD Implant As
- #linear oxide anneal
- deposit nitride spacer
- etch oxide/nitride spacer
- NSD implant: As, P
- step NSD RTA anneal (*)
- step metal deposit

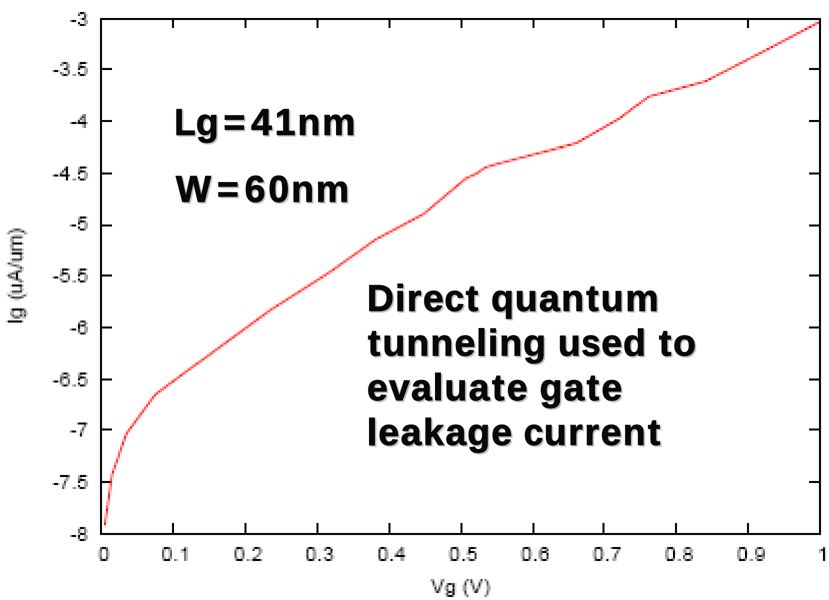
Simplified steps with fewer thermal cycles for the purpose of studying dopant diffusion/segregation

(*) RTA simplified by 900 C anneal

Simulation studies

- Comparison of 4-plane with 8-plane simulation (physical trend unchanged).
- Comparison of quantum mechanical model and classical model.
- Comparison of effect of thermal cycles on threshold behavior.
- Study of Vth at different channel widths.





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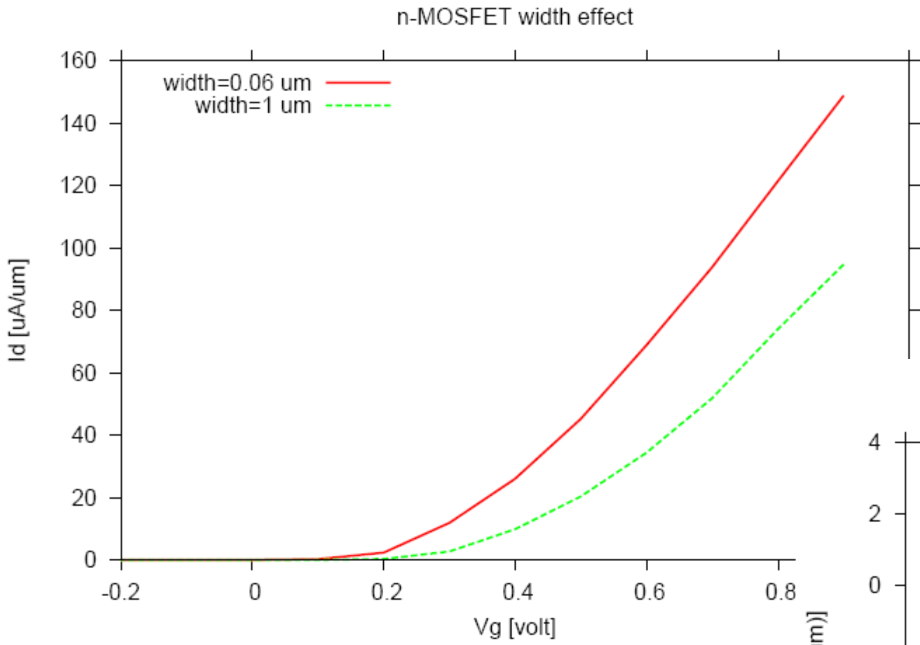
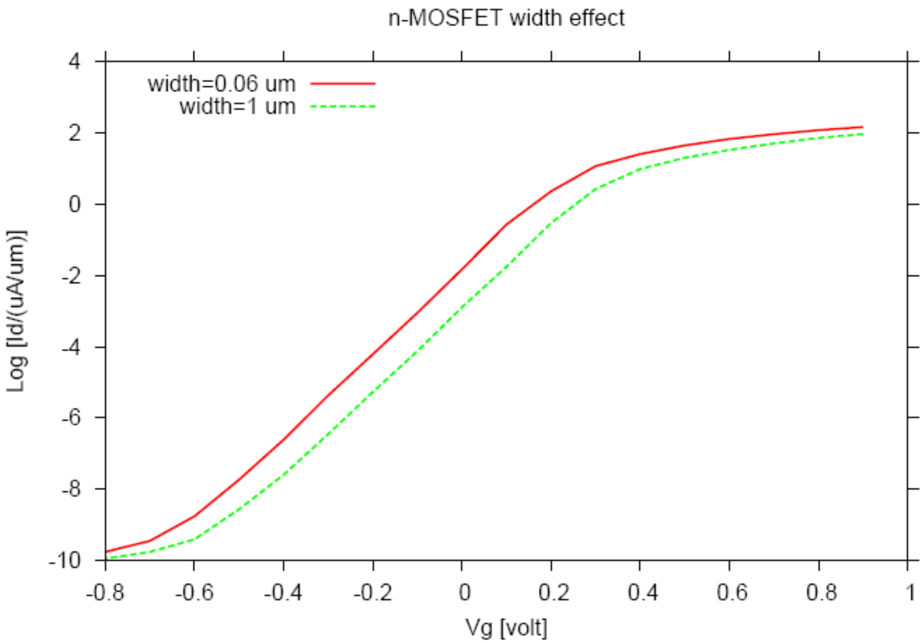
Simplified process steps (4-planes)



With fewer thermal cycles, no significant diffusion/segregation in width direction is observed. Dopant profiles are unchanged for different widths.

Electrical simulation shows reduced Vth as width is reduced.



Explanation for shift in Vth for simplified process (3D geometric effect)

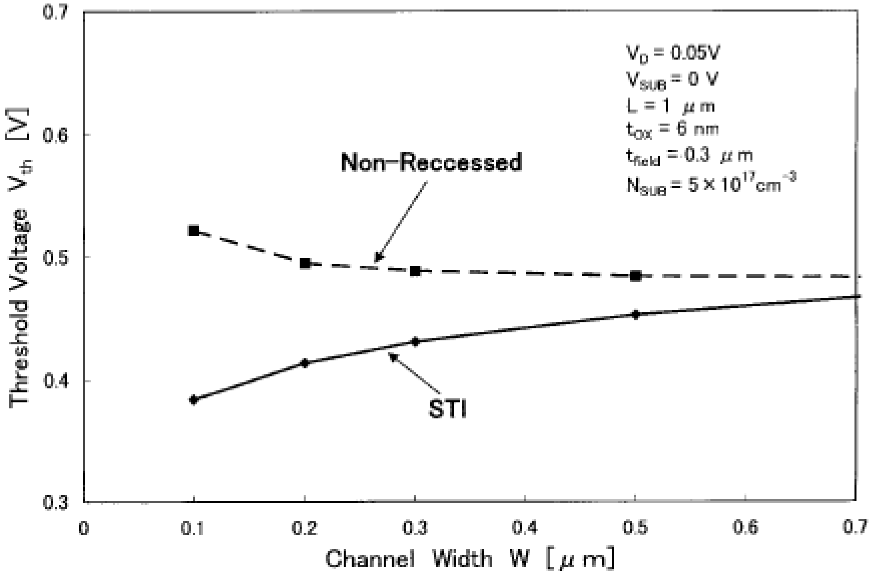
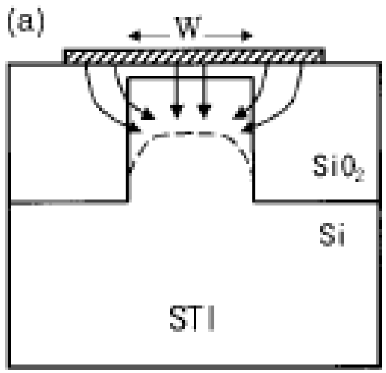


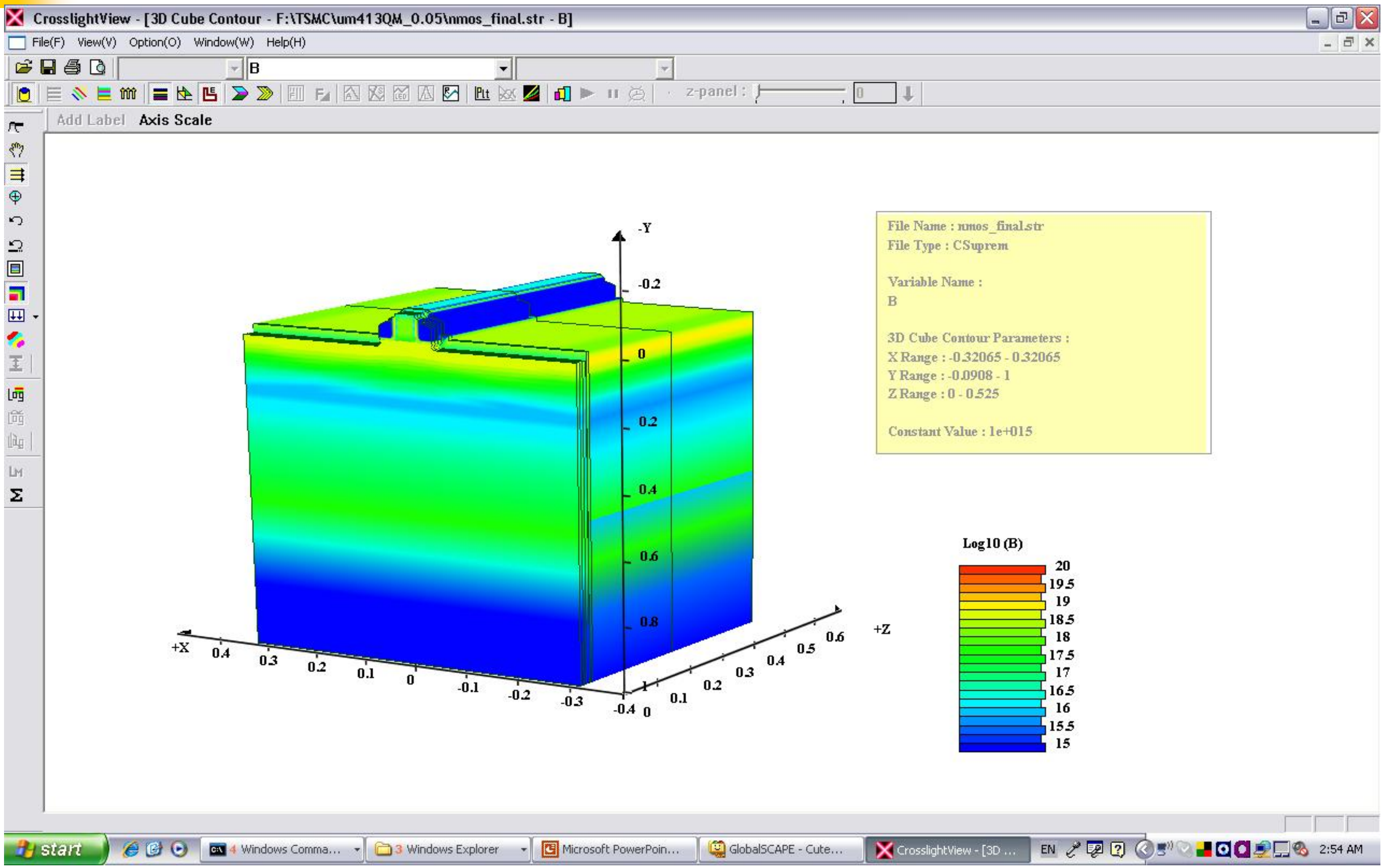
Fig. 2. Three-dimensionally simulated V_{th} as a function of W.



N. Shigyo, T. Hiraoka / Solid-State Electronics 43 (1999) 2061-2066

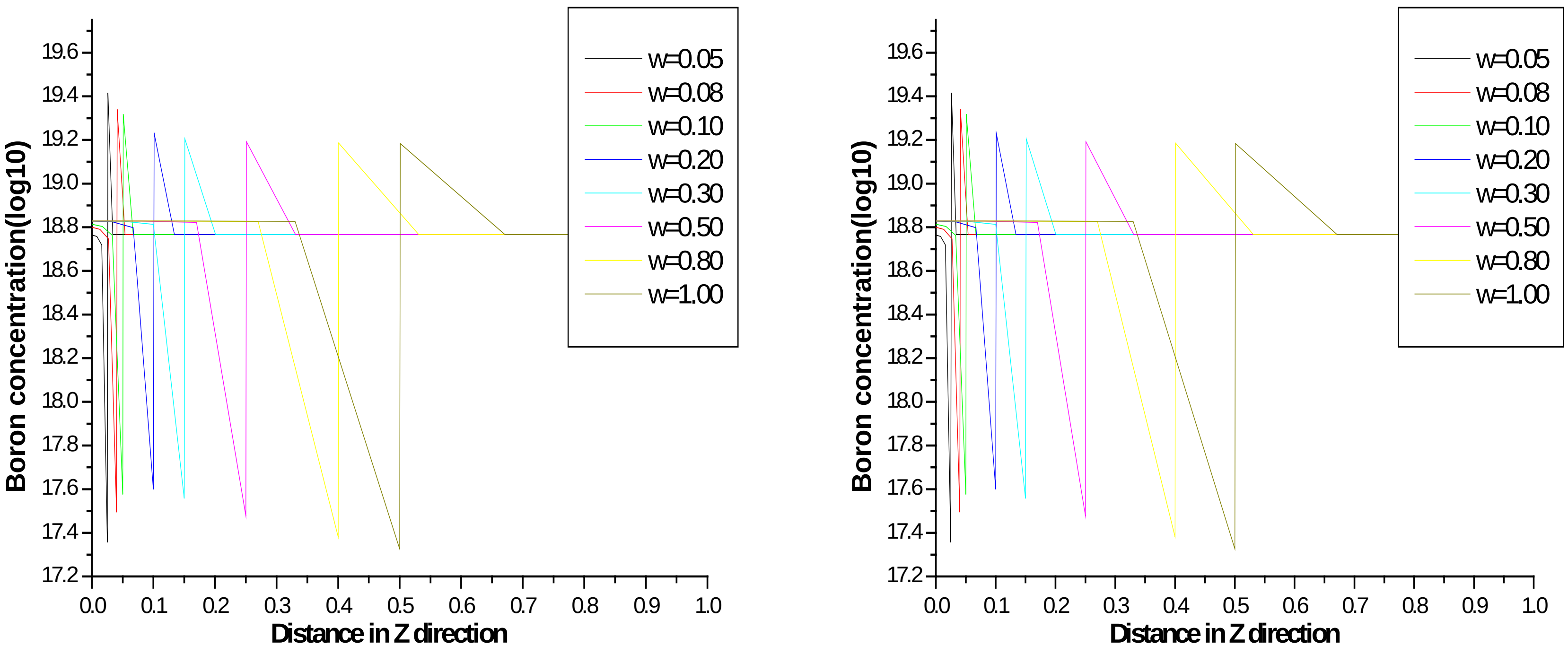
Explanation: assuming no change in dopant distribution, additional fields from the sides make it easier to turn on the device for narrower device: downward shift in Vth for narrower STI device.

Boron distribution (3D,w=0.05)



Use of full thermal cycles causes strong variation in dopants along z-direction.

Boron width distribution below gate



Cut at x=0 y=50 A Lgate=0.0413 um

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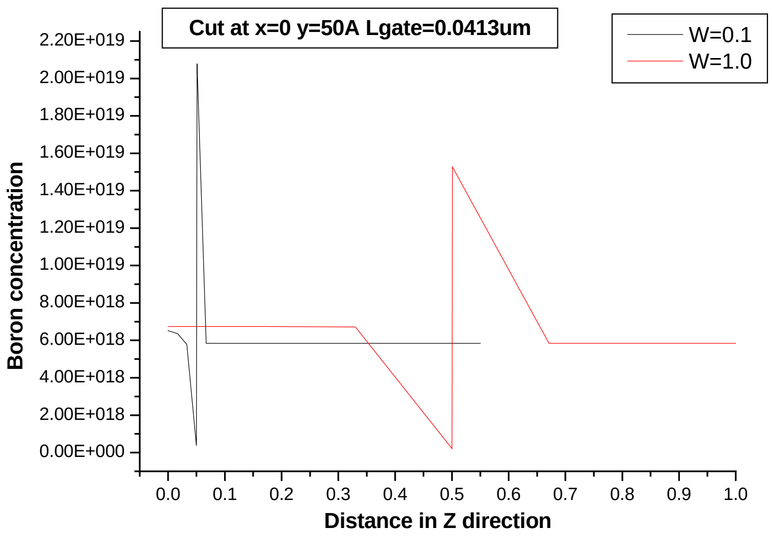
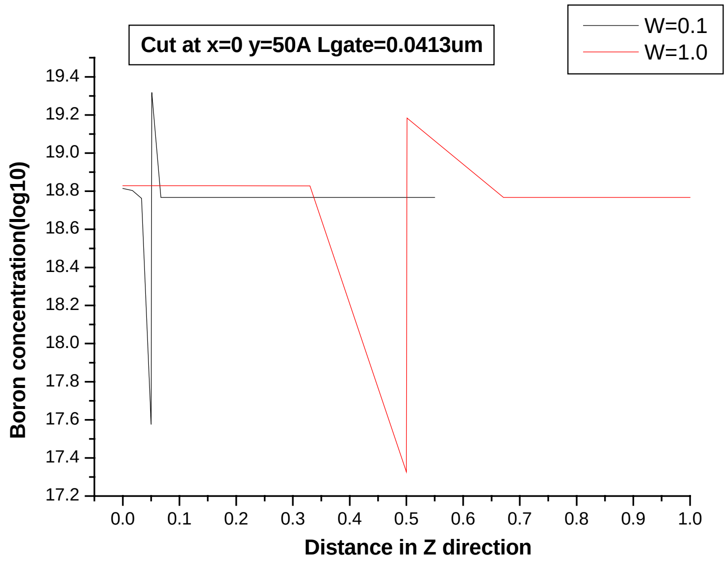
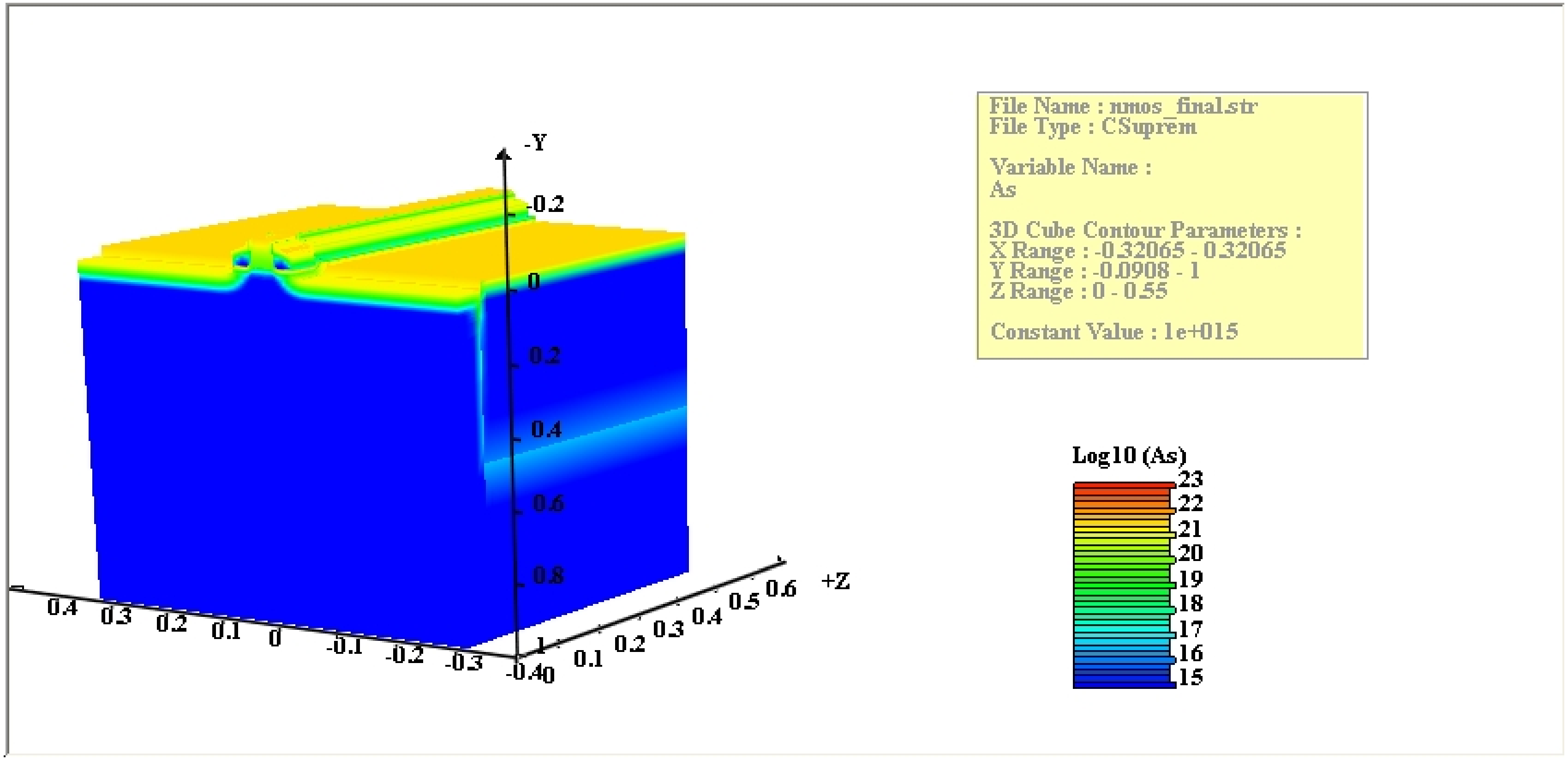
Boron width distribution (w=0.1, 1)



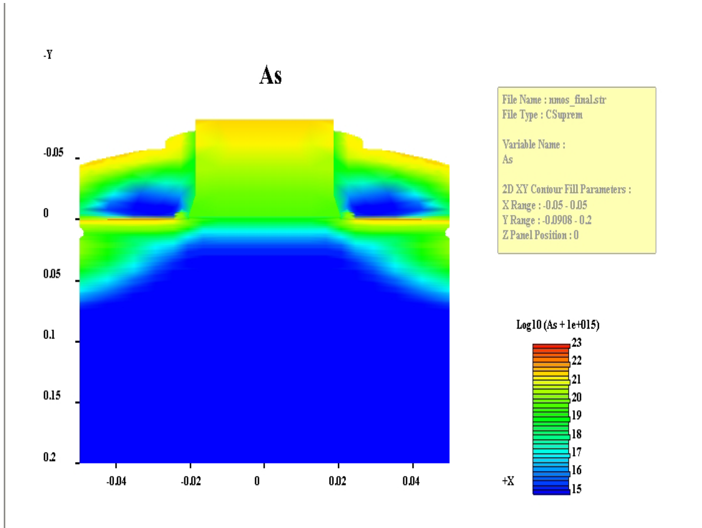


Cut at x=0 y=50 A Lgate=0.0413 um

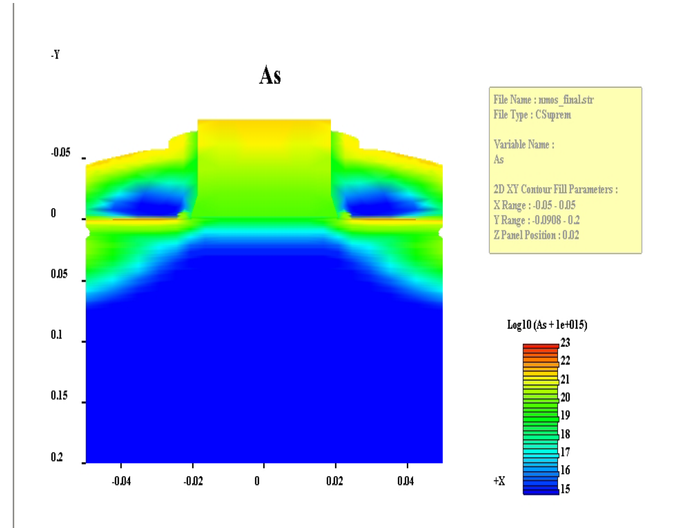
Arsenic distribution (3D,w=0.1)



Arsenic distribution (w=0.1,channel portion)

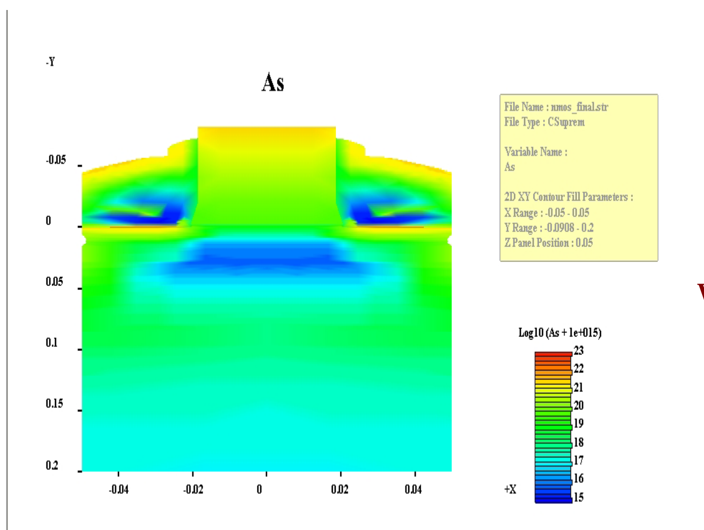


W=0.10 um z=0.0 As



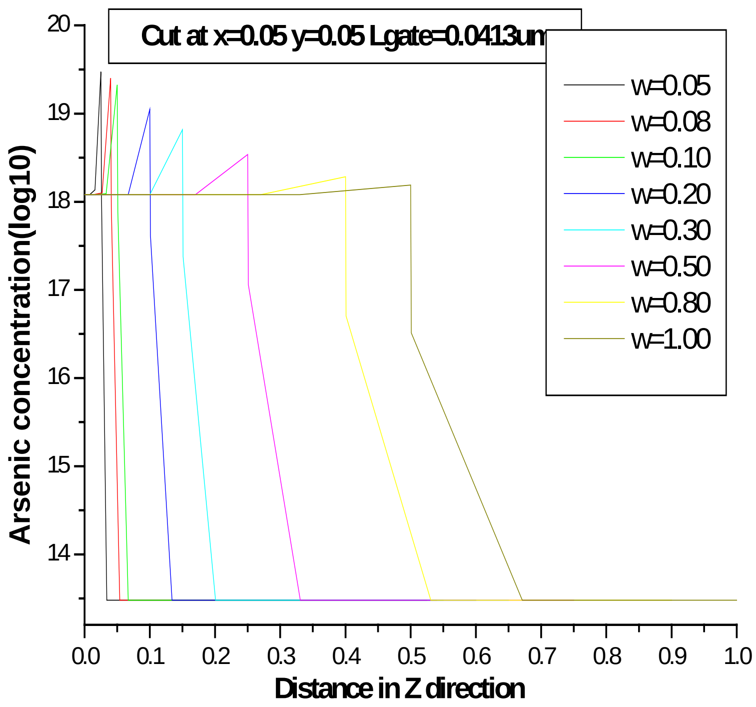
W=0.10 um z=0.02 A

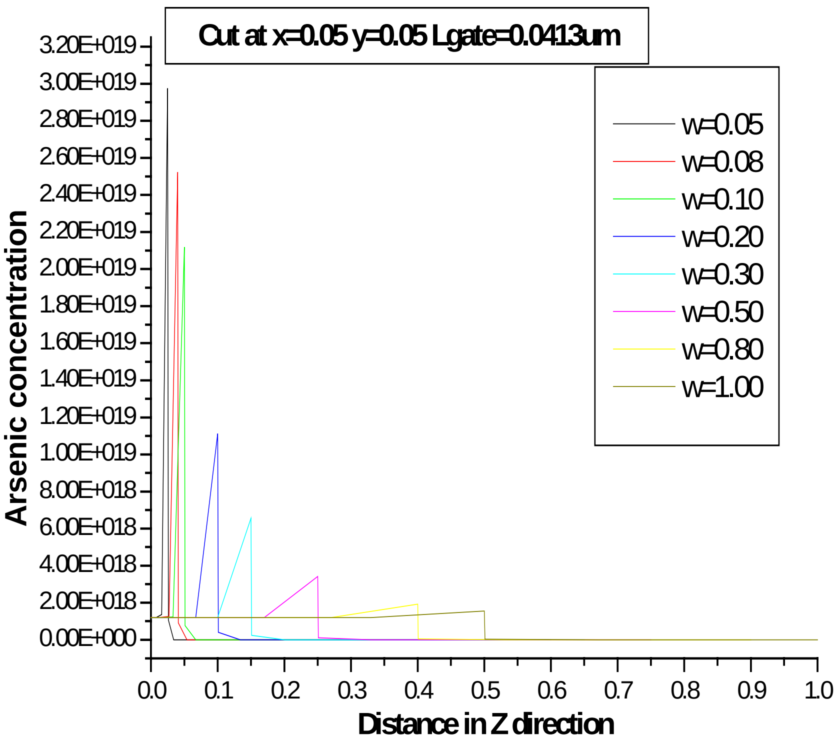
Remark: please note the difference between z=0 and z=0.05



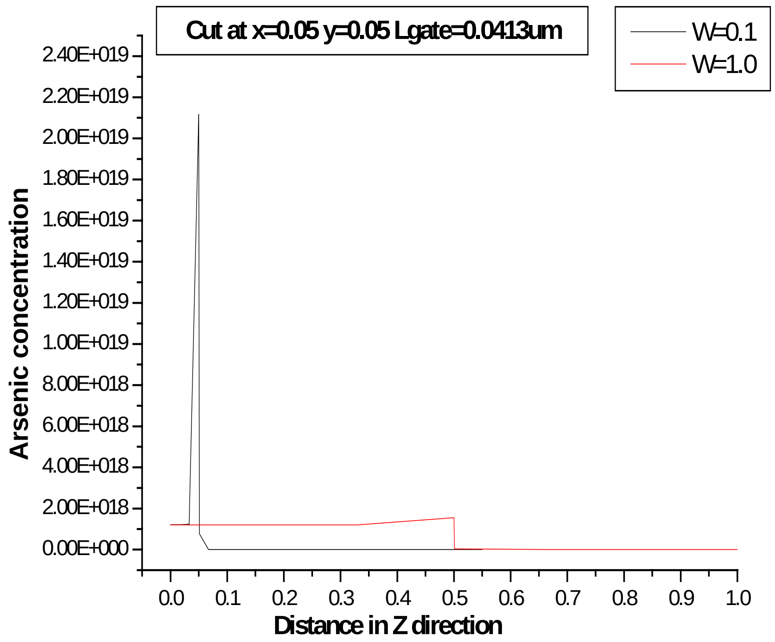
W=0.10 um z=0.05 As

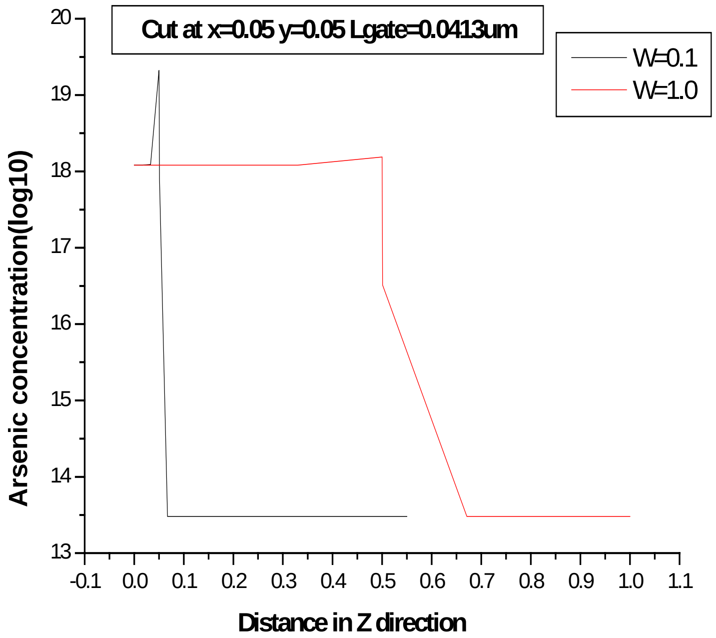
Arsenic width distribution (near S/D)





Arsenic width distribution (w=0.1,1)





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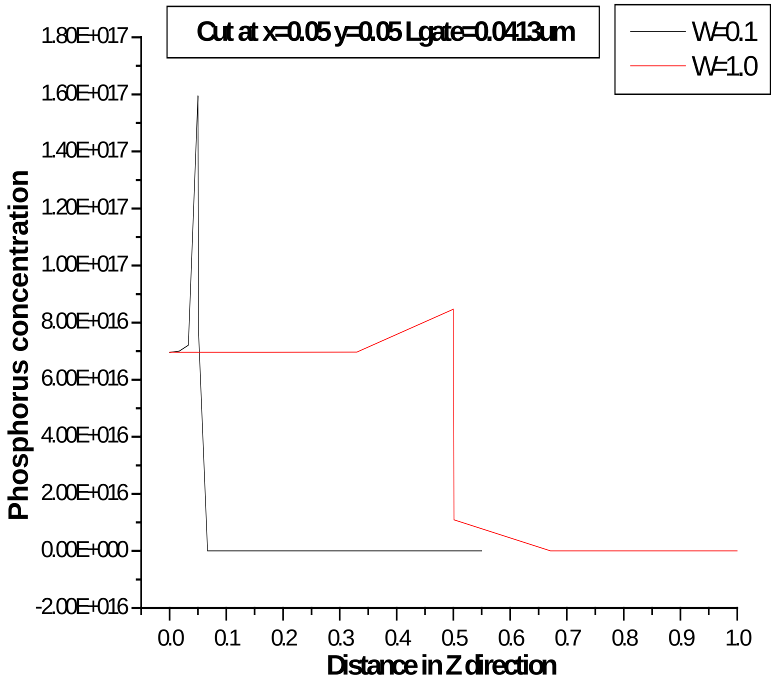
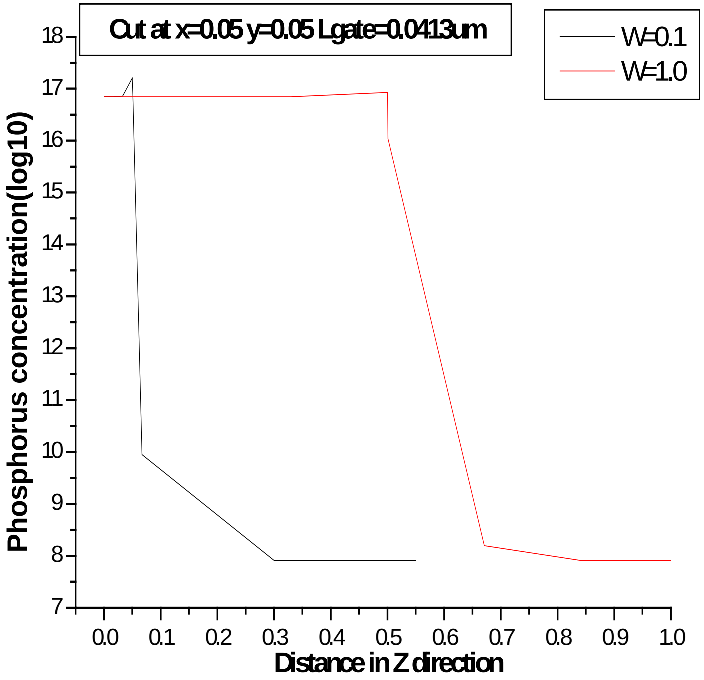
Phosphorus width distribution (near S/D) (w=0.1,1)





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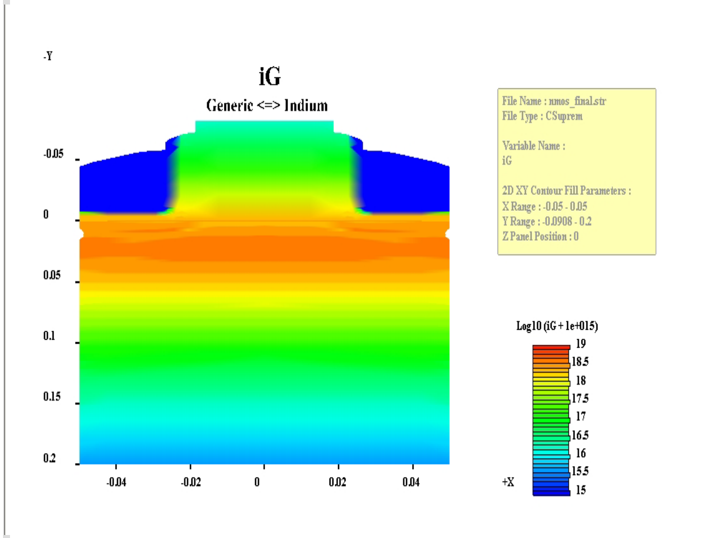
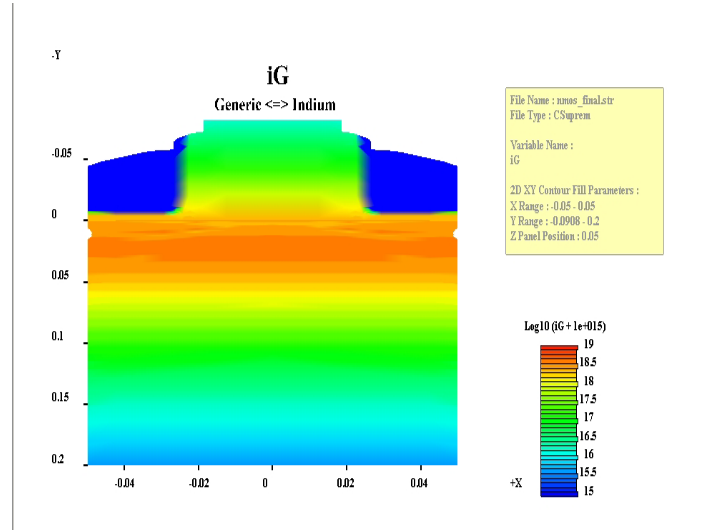
Indium distribution (w=0.1, channel portion)



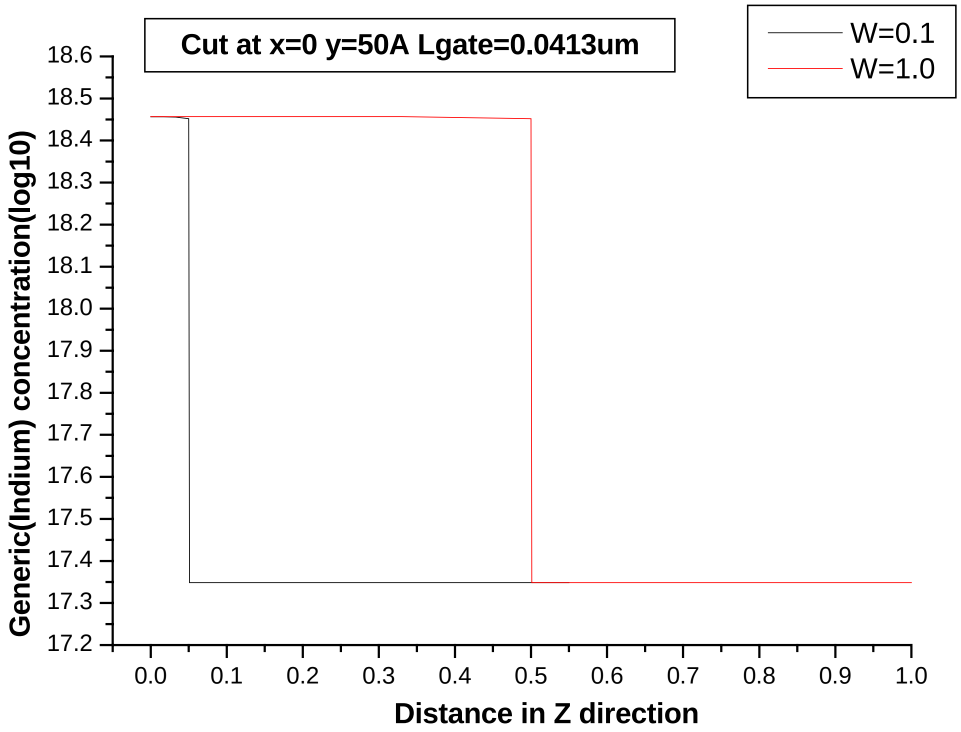
W=0.10 um z=0.0 Ge



W=0.10 um z=0.05 Ge

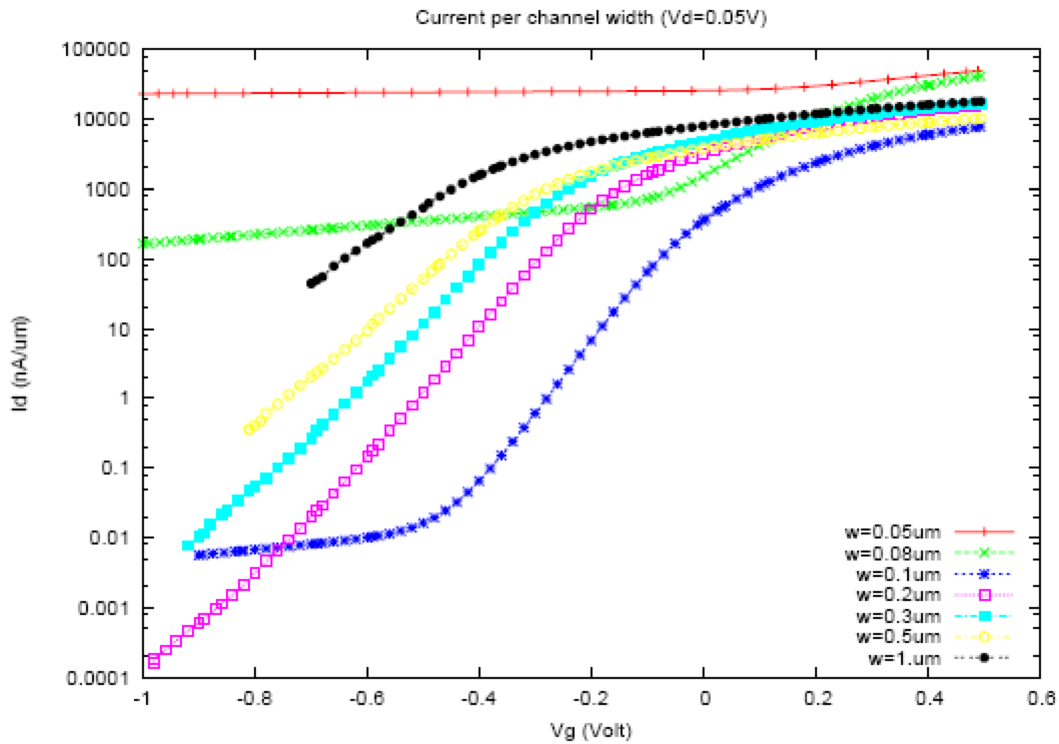
Remark: indium is defined as "generic" dopant

Indium width distribution (w=0.1,1)



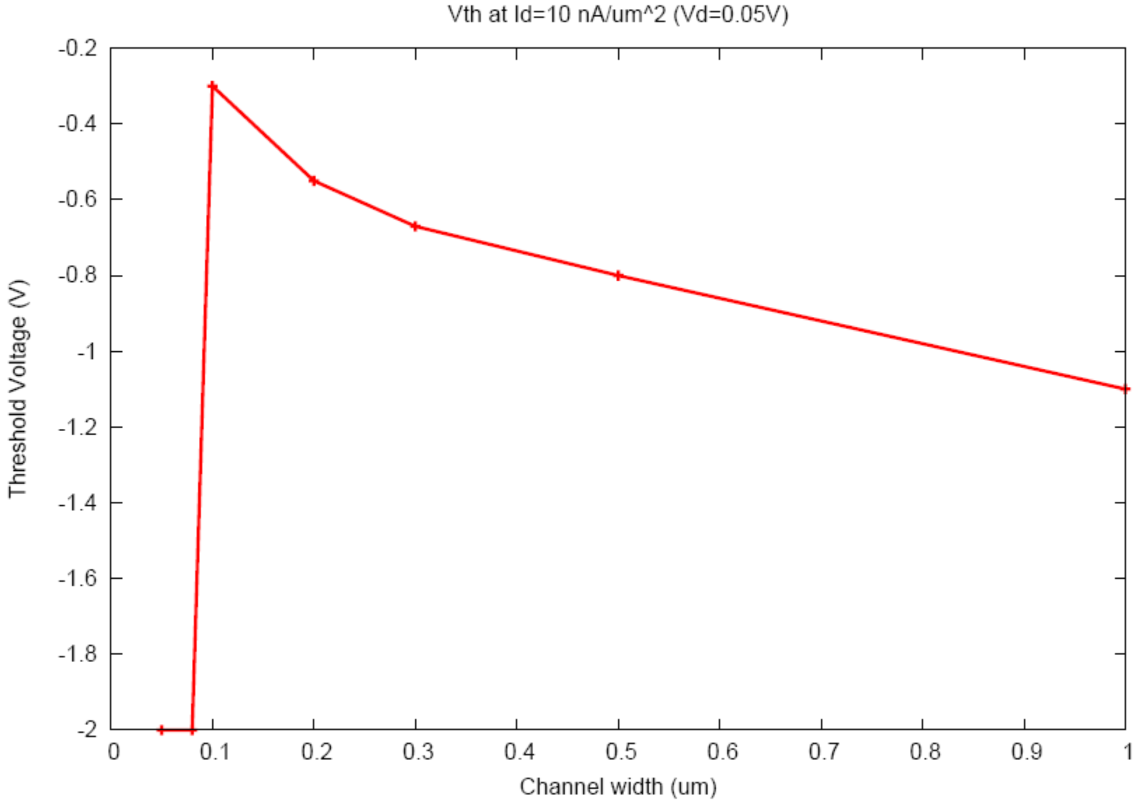
Remark: segregation model for Indium is not enabled in this study and thus total lack of 3D/width effects was observed.

Id-Vg at Vd=0.05 Volt (log plot)



Remark: smaller gate width tends to cause large subthreshold current, similar to one of the short channel effects. Explanation: too narrow a gate width prevents gate controlling potential from reaching deep into the channel.

Threshold voltage behavior



Remark: behavior for <0.1 um not well defined due to large subthreshold current. For nano-MOSFET, Vth behavior is totally different than its longer gate counterpart due to difference in thermal process and 3D geometric effects.

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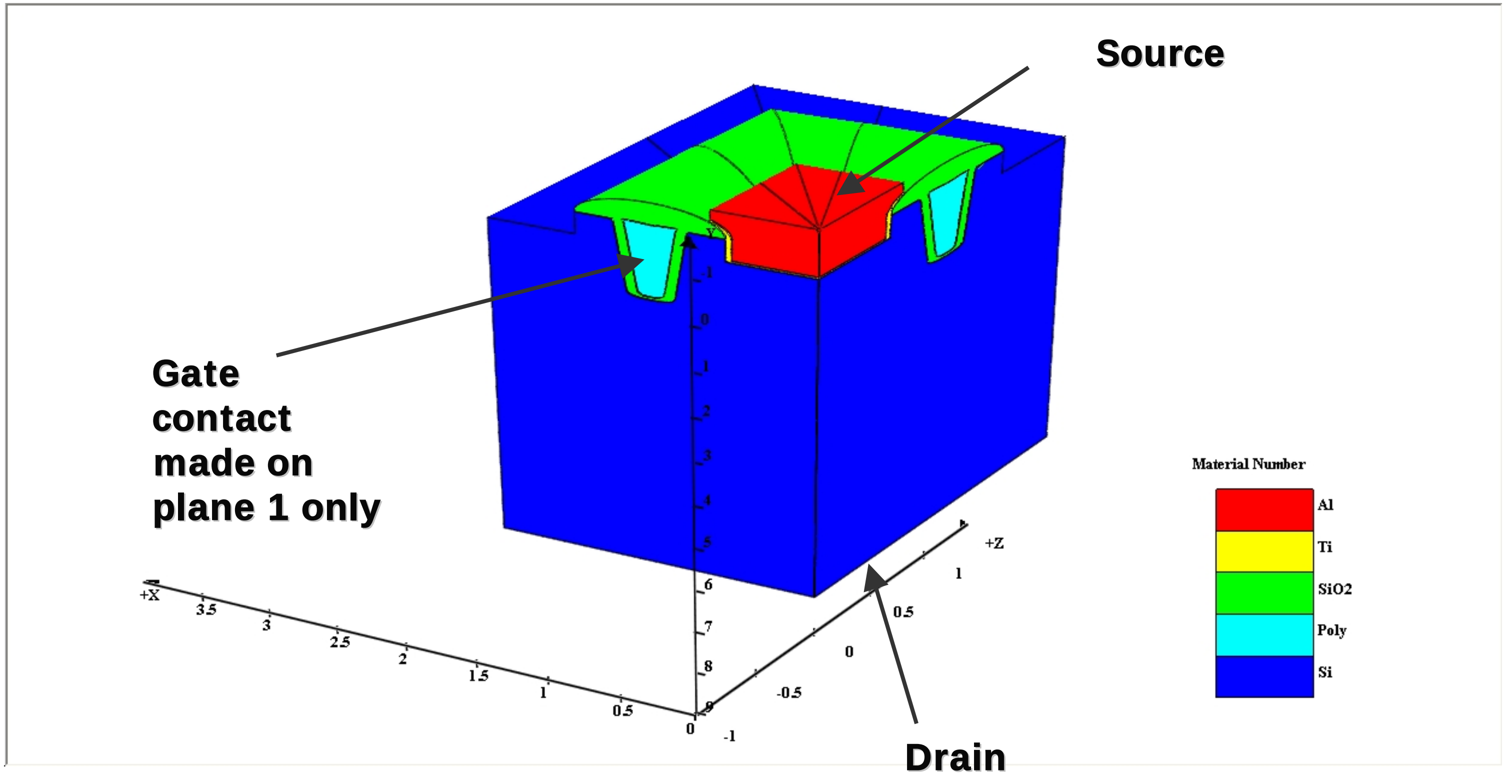
Case study: square-trenched UMOS



Use rotated mesh planes so that the U-shaped trench/GOX can be accurately defined for all parts of the 3D structure which is to be compared with pure 2D simulation of plane 1.

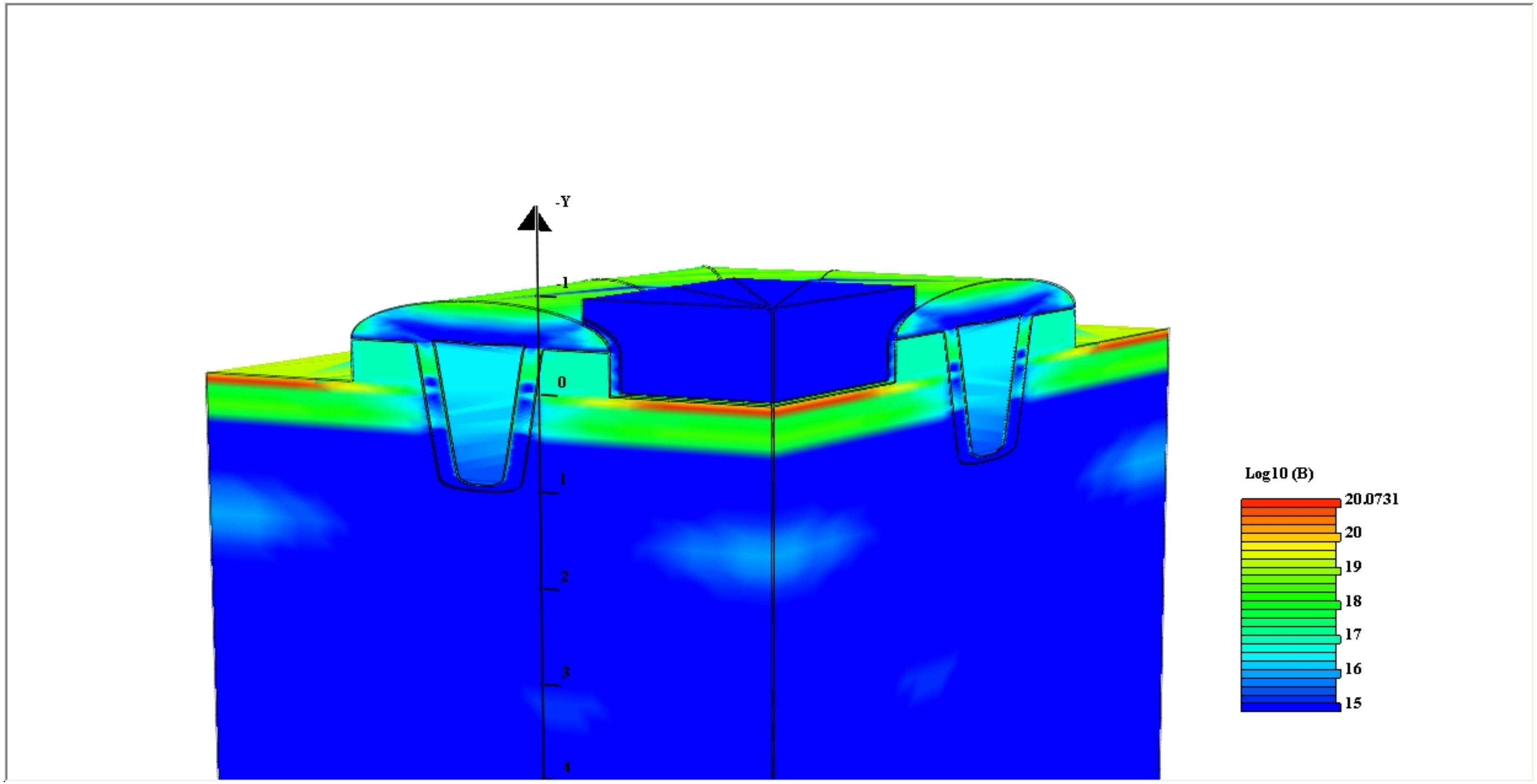
Using a typical UMOS process flow

- epi-growth; anneal with dry oxidation
- etch oxide for trench definition
- RIE (iso+vertical) etch silicon reaching desired trench depth
- anneal with wet oxidation reaching final shape of trench; remove oxide
- anneal with dry oxidation for GOX growth
- deposit poly to fill-in the trench
- implant boron for p-body; anneal for body drive-in
- deposit/pattern photoresist for n-body implant
- implant arsenic for n-body; anneal for n-body drive-in
- deposit and pattern thick oxide
- etch silicon to make step-shape for source contact
- implant boron and BF2
- etch and shape top oxide layer; deposit Ti for source contact
- final anneal
- deposit Al; etch and pattern metal for source contact
- export mesh and dopant to APSYS for electrical simulation

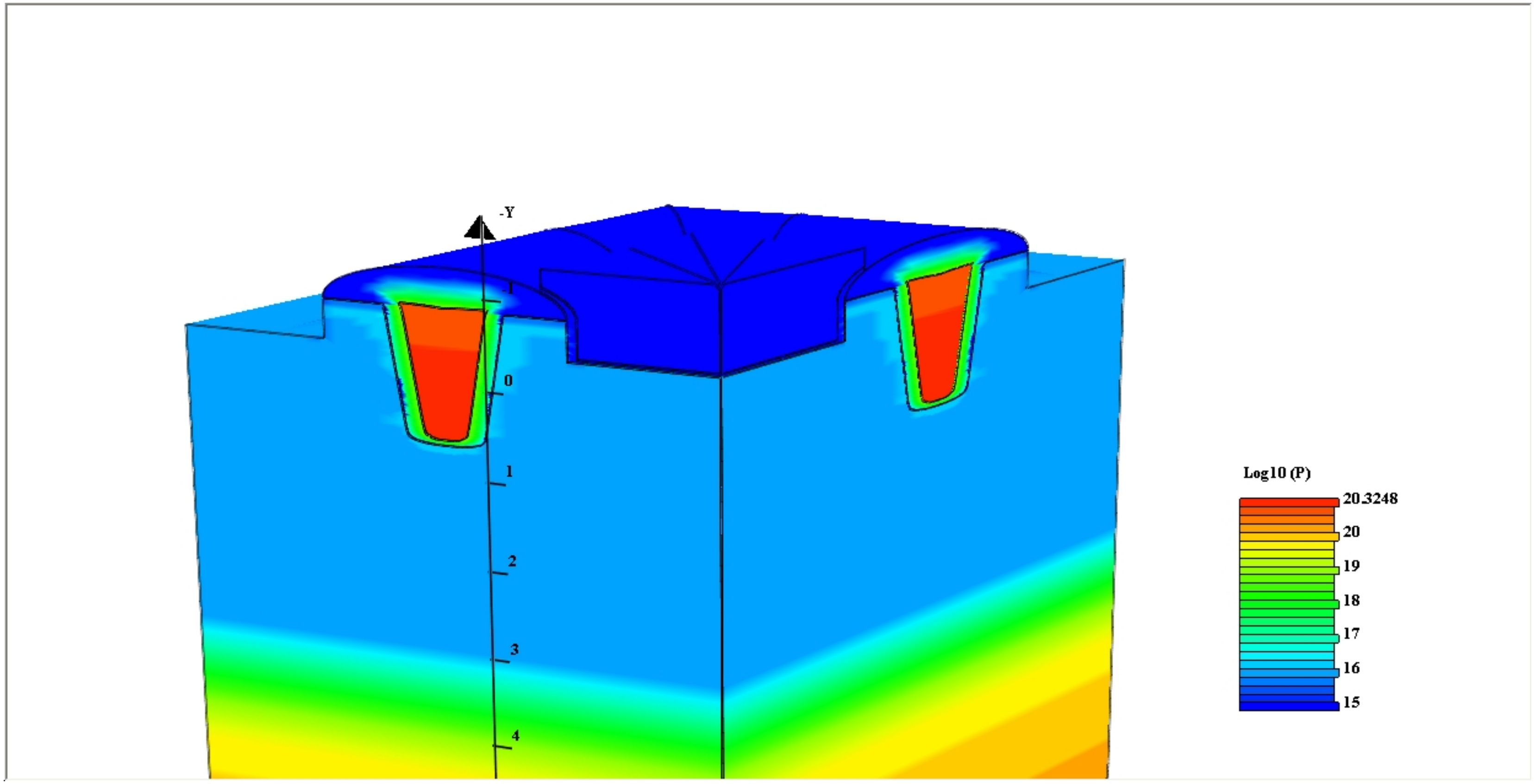
Simulation studies

- Use the same process input decks as for 2D simulation for all planes of the 3D structure.
- Enable (full) or disable (quasi) 3D inter-plane diffusion to study its effect on final electrical characteristics.
- Use same full-3D APSYS electrical simulation for 3D structures grown by full-3D and quasi-3D diffusion.
- Compare electrical behavior with pure 2D simulation to see the trench corner effect.

Final boron distribution



Final phosphorous distribution



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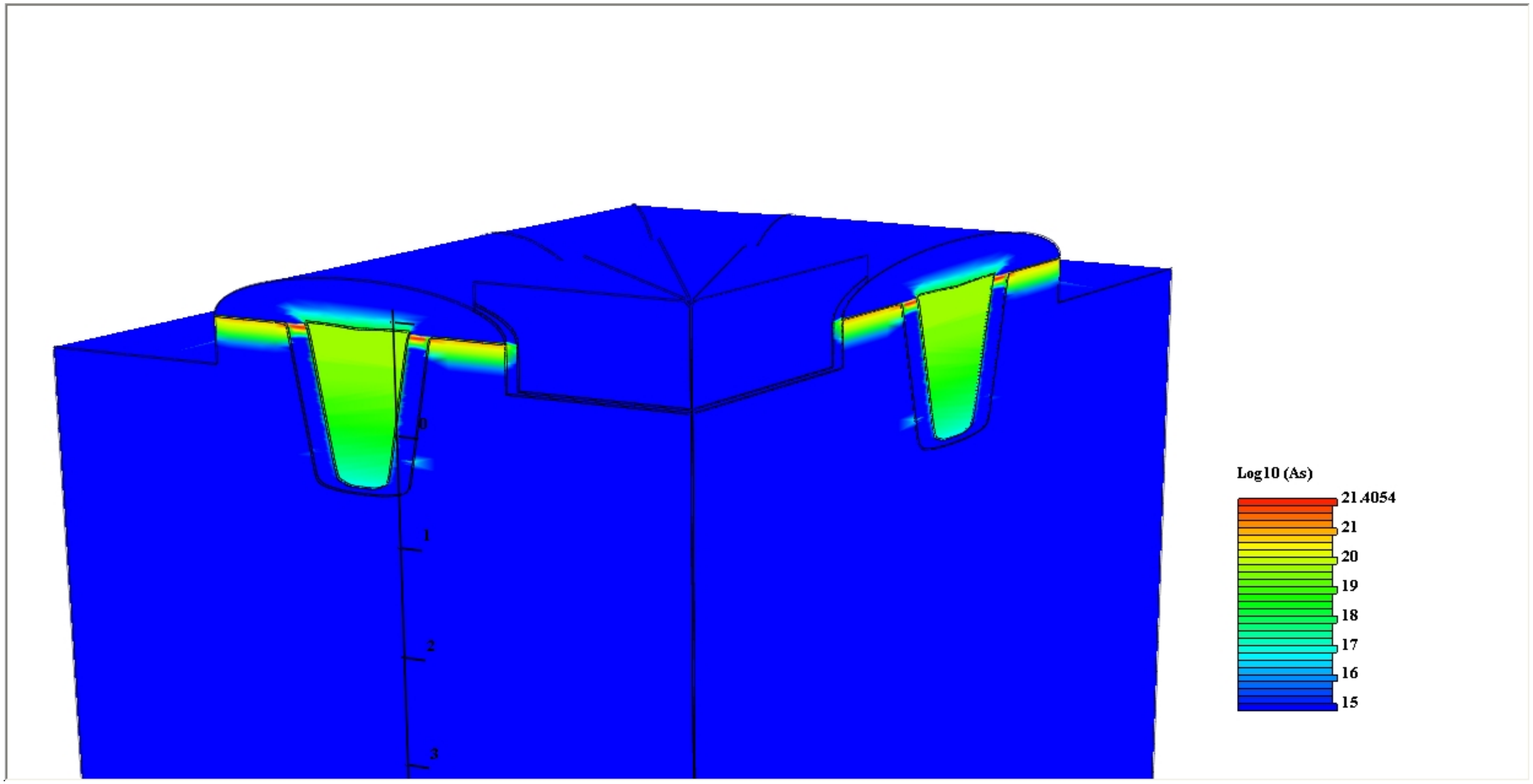
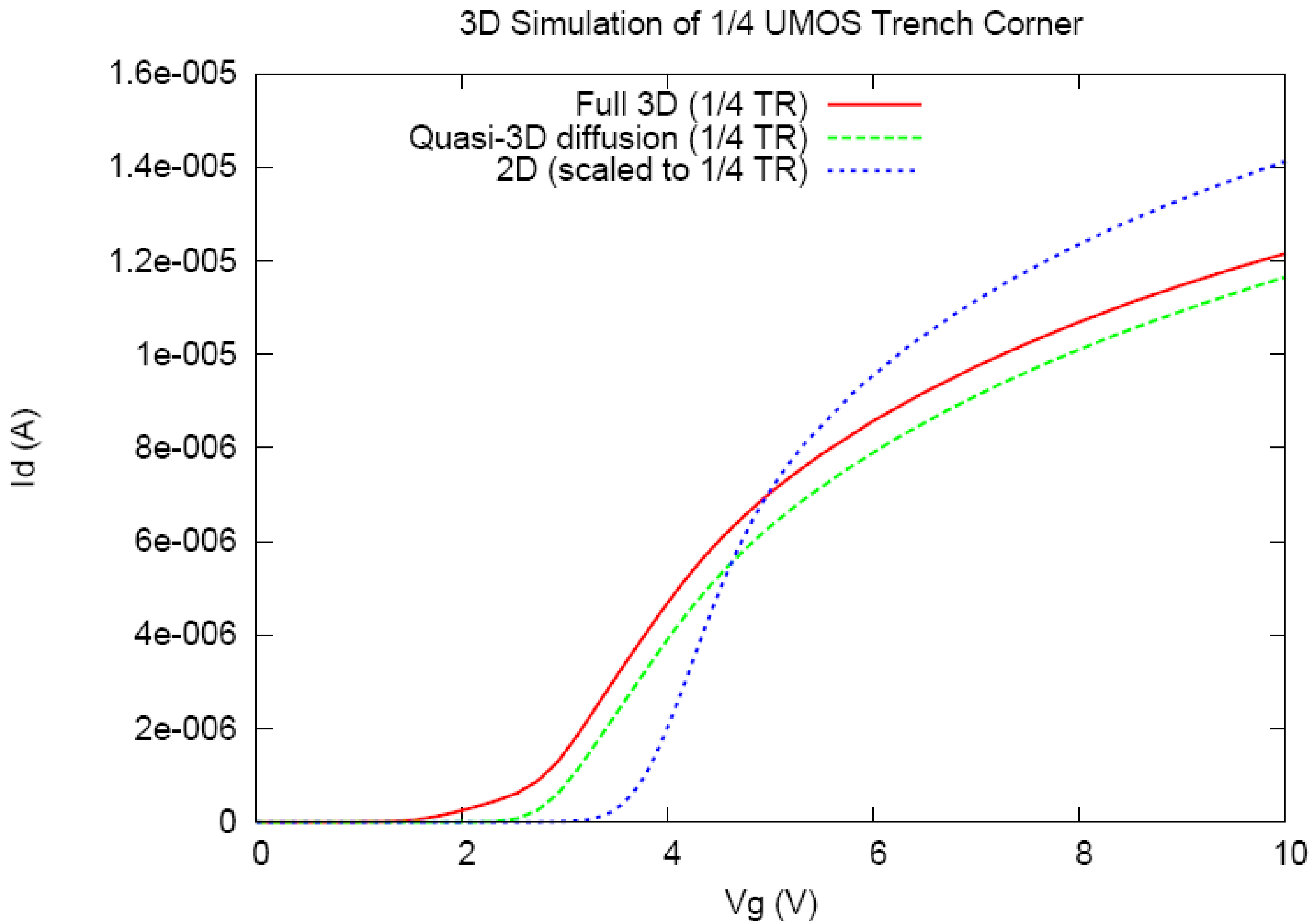
Final arsenic distribution

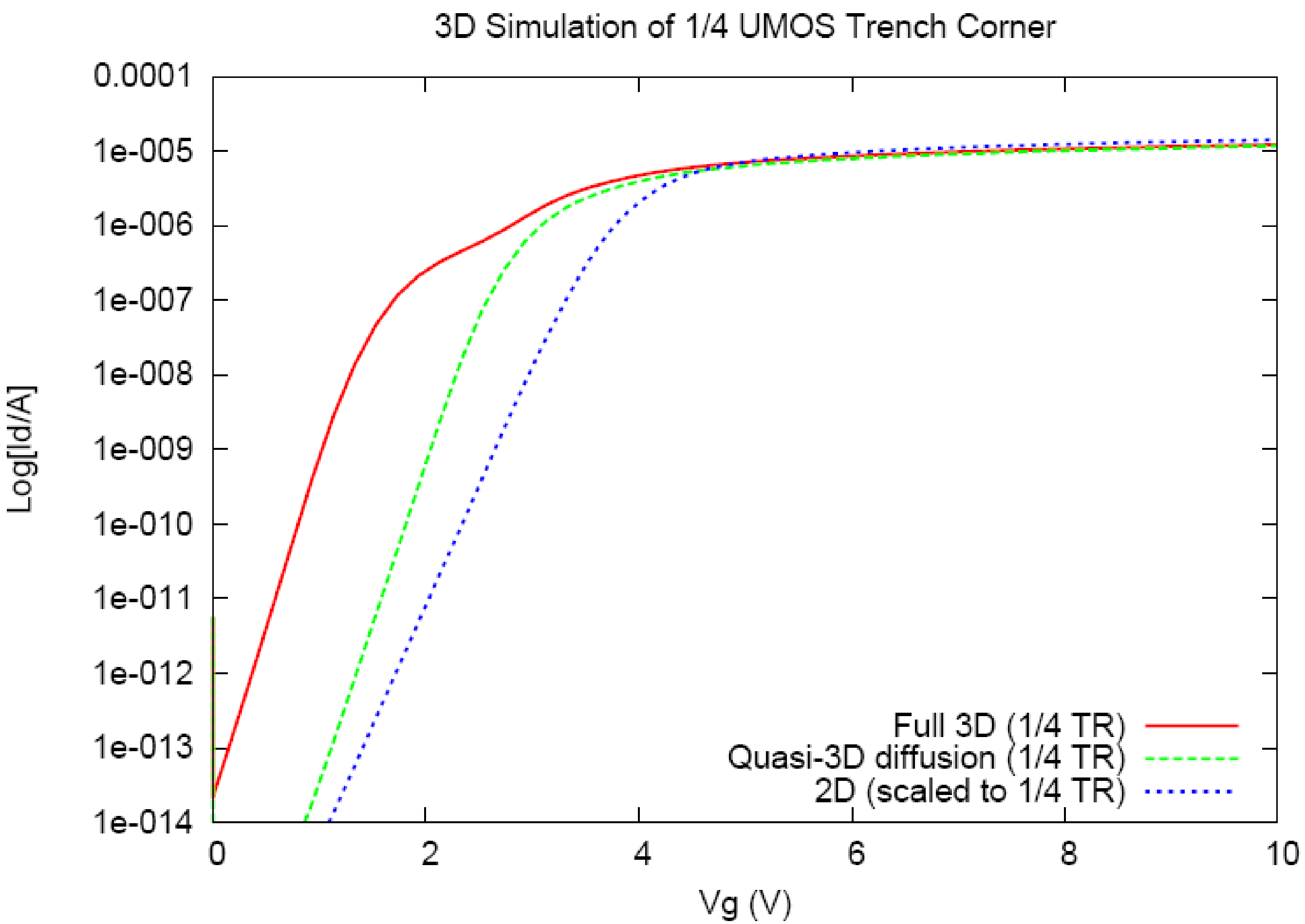


Comparison of Id-Vg



Remark: substantial difference between 2D and quasi-3D diffusion structure indicates large 3D geometrical effect.

Comparison of threshold behavior



Remark: significant difference between full 3D and quasi-3D diffusion indicates the importance of 3D dopant diffusion caused by the trench corner.

Conclusions

- For STI confined MOS dopant diffusion in width direction is caused by SiO_2/Si interface segregation.
- For larger HV MOSFET, 3D diffusion and narrow gate side-field cause downward shift in Vth as width is reduced.
- For typical process flow of nano-MOSFET, Vth increases with decreasing width for W>0.1 um.
- For square-trenched UMOS, both geometrical and 3D diffusion effects cause downward shift in Vth as square size is reduced.